

MODELING AND SIMULATION OF
FAULT TOLERANT PROPERTIES OF
QUANTUM-DOT CELLULAR AUTOMATA DEVICES

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ABSTRACT

THESIS: Modeling and Simulation of Fault Tolerant Properties of Quantum-dot Cellular Automata Devices

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I present a theoretical study of fault tolerant properties in Quantum-dot Cellular Automata (QCA) devices. The study consists of modeling and simulation of various possible manufacturing, fabrication and operational defects. My focus is to explore the effects of temperature and dot displacement defects at the cell level of various QCA devices. Results of simple devices such as binary wire, logical gates, inverter, cross-over and XOR will be presented. A Hubbard-type Hamiltonian and the inter-cellular Hartree approximation have been used for modeling the QCA devices. Random distribution has been used for defect simulations. In order to show the operational limit of a device, defect parameters have been defined and calculated. Results show fault tolerance of a device is strongly dependent on the temperature as well as on the manufacturing defects.

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John Michael Padgett: 1948-2006

Next I would like to thank my advisor, Dr. Mahfuza Khatun, for her wisdom, encouragement, and patience. She maintained positive encouragement through countless code problems and a lengthy thesis timeline. Professors like her are what make Ball State a great learning environment.

I would also like to thank Ball State University for letting me hang around for so many years. The support and encouragement of the faculty and staff never ceased to amaze me. I entered the program thinking a small physics department would not be right

for me and I actually tried to escape to Purdue. After seeing Ball State's high teacher to student ratio, and close personal environment, I do not feel any other department could have been better for me. The teaching assistantship was also a nice bonus. Without the financial support of the university I would not have been able to continue my education.

I would like to thank the previous students that worked on the QCA project at Ball State. Gabriel A. Anduwan, Melissa K. Hendrichsen, and Travis J. Barclay all worked with the same code I used. Although I never worked directly with them, I was able to benefit from their progress in the field and I learned a great deal from their theses. Mike Kuntzman is the only student I worked with directly on QCA. He introduced me to the code and the Beowulf Cluster. Mike also produced some of my results in Chapter 3. He worked as an undergraduate, so I did not have a thesis to reference, but he did contribute to the QCA research.

Lastly, I would like to thank my fiancé, Deidre N. Hopkins. She stood by me through the lengthy writing process. She also offered strong encouragement to finish the thesis and move on from student to employee. If it were not for her, I may still be tinkering with the code to test more devices, or to get more refined results.

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CHAPTER 1: INTRODUCTION

1.1. Overview

In the present research project, a unique paradigm for computation has been studied. The new Quantum-dot Cellular Automata (QCA) devices require investigation to determine their feasibility as a replacement for current Complementary Metal-Oxide-Semiconductor (CMOS) technology. The use of quantum mechanical properties for computation promises faster processing at a greatly reduced size [1].

Quantum-dot Cellular Automata devices are smaller, faster, and consume less energy than existing CMOS (Silicon-based) technology. QCA allows for propagation of a signal with no current, so there is low power consumption and low heat dissipation [1, 2]. The signal is propagated through Coulomb force interactions and utilizes bi-stable polarization states so Boolean logic still applies.

To utilize traditional computation techniques, QCA must have two polarization states to represent a “zero” or a “one.” This allows the use of traditional Boolean logic. Many quantum computation schemes incorporate more than two bits, which creates the additional trouble of redesigning all conventional computational methods to utilize the additional bits. QCA is a bistable system, so it allows for the increased speed, reduced size, and the same basic binary programming as current CMOS technology.

1.2. Fault Tolerant Properties of QCA

Before QCA can be adopted as a computational process, fault tolerances need to be investigated. As with all manufactured devices, fault tolerances need to be investigated to see how much of a defect can be present while still functioning properly. Recently, several researchers have investigated some fault tolerant properties and characteristics [3-7]. The faults studied fall into two categories: operational faults, and manufacturing faults.

Operational faults are based on the environment the QCA device will operate in. This includes temperature effect, stray charge, etc. Temperature is currently the main operational fault of study by the research group at Ball State University [8-10].

Manufacturing faults focus on either the design of the device, or on the fabrication of the device. Design defects are associated with the computational layout of the cells, whereas manufacturing defects are derived from the creation of the cells. Since QCA operates on such a small scale, very slight defects could cause the device to fail, so the manufacturing process must be very precise. Manufacturing defects need to be thoroughly studied before QCA can be employed as a new mode for computation. These faults will be tested and discussed further in Chapters 3 and 4.

1.3. Thesis Layout

In Chapter 2, the basic structure and theoretical operation will be reviewed. Chapter 3 will cover several basic QCA devices and discuss their simulation results. Chapter 4 will focus on the Exclusive OR (XOR) gate, which is much more complex than any of the basic devices presented in Chapter 3. Also, clocking will be introduced in

Chapter 4. Chapter 5 will conclude the thesis by summarizing, and provide direction for future QCA work.

CHAPTER 2: A REVIEW OF LITERATURE

2.1. Introduction

In this chapter, the background of the current thesis work is reviewed. The concept of QCA was first published in 1993 [11], and much work has been done in the past sixteen years. To understand the current thesis work, some of the past concepts need to be reviewed.

2.2. The QCA Model

As mentioned in Chapter 1, a QCA cell can hold binary information in the form of polarization states. To hold two polarization states, each cell is a square with quantum dots in each corner. A QCA cell contains four or five dots as shown in Fig.2.1(a) and (b) respectively. The five-dot system utilizes a central dot to aid in tunneling for polarization transitions. Each cell contains two excess electrons which use Coulombic interactions to anti-align within the cell. The electrons are free to tunnel between dots within the cell, but are not permitted to tunnel between neighboring cells. This creates two stable states in which the cell is most probable to be in, as shown in Fig.2.1(c). The two states are designated as +1 or -1, which can replace the traditional binary 1 and 0. The assignment of positive and negative to the polarization states has no physical significance, it was an arbitrary decision made in QCA's infancy.

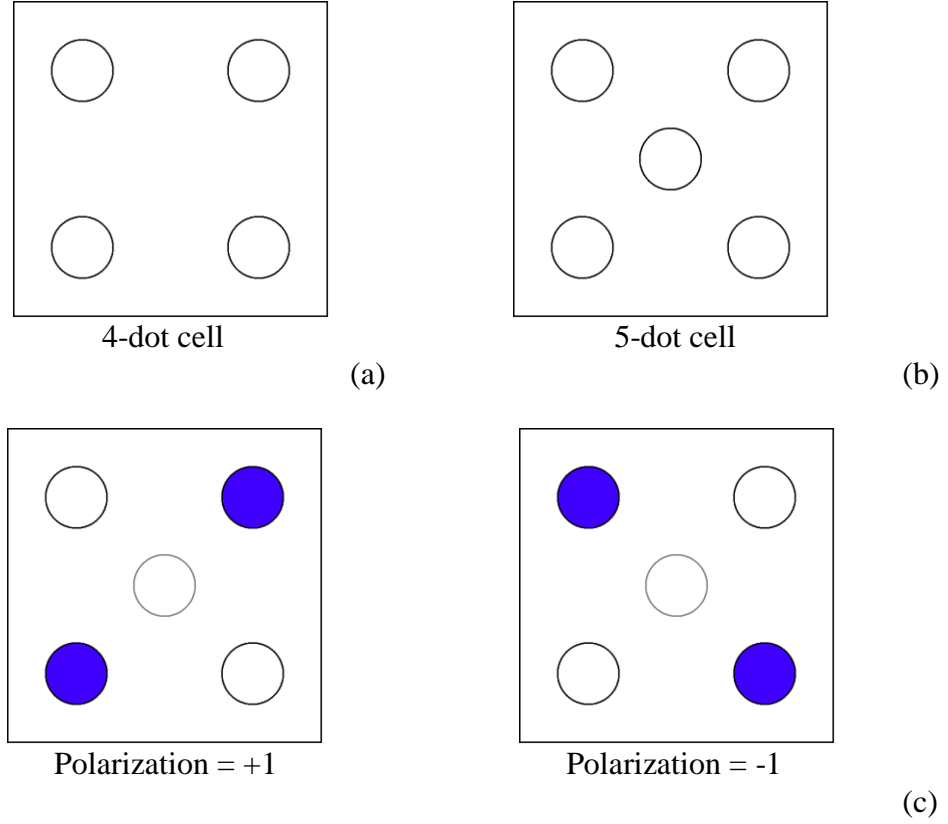


Figure 2.1: The QCA cell structure for (a) a 4-dot system, (b) a 5-dot system, and (c) their two ground state polarizations.

Although the excess electrons cannot escape their cells, they can interact electrostatically with neighboring cells. When two cells are brought close enough together, they will interact to align to the same polarization configuration. Thus if a chain of cells are placed in a row, a binary wire can be created [12], which will be discussed in Chapter 3.

2.3. Hamiltonian

To simulate a QCA system, a computational model needs to be created. Most importantly, it needs to be meaningful and feasible for modern computers to calculate in

a reasonable amount of time. With these constraints, the cell Hamiltonian for a single isolated cell is given by [1, 2]:

$$\hat{H}_0^{cell} = \sum_{i,\sigma} E_0 \hat{n}_{i,\sigma} + \sum_{i>j,\sigma} t_{i,j} (\hat{a}_{i,\sigma}^+ \hat{a}_{j,\sigma} + \hat{a}_{j,\sigma}^+ \hat{a}_{i,\sigma}) + \sum_i E_Q \hat{n}_{i,\uparrow} \hat{n}_{i,\downarrow} + \sum_{i>j,\sigma,\sigma'} V_Q \frac{\hat{n}_{i,\sigma} \hat{n}_{j,\sigma'}}{|\vec{R}_i - \vec{R}_j|}. \quad (2.1)$$

The first term calculates the onsite energy associated with the confinement of an electron on a particular site or quantum dot, where E_0 ($= 130.6$ meV for silicon semiconductor) is the onsite energy and $\hat{n}_{i,\sigma}$ is the number operator for an electron at site i with spin σ .

The second term calculates the tunneling energy. The $t_{i,j}$ term is the energy associated with the tunneling of electrons from site i to j , which is about 0.3 meV for neighboring dots in a silicon cell. As spacing is increased, $t_{i,j}$ will go to zero. The annihilation ($\hat{a}_{i,\sigma}$) and creation ($\hat{a}_{i,\sigma}^+$) operators destroy an electron at site i or j with spin σ , and recreate it at a different site, respectively. The third term calculates the spin energy. E_Q ($= 846$ meV) is the energy for two electrons with opposite spin to occupy the same dot. The last term is for the Coulombic potential energy. V_Q ($= \frac{e^2}{4\pi\epsilon}$) is a fixed parameter based on fundamental constants and the dielectric of the material. It represents the Coulombic potential energy between the two electrons within the same cell.

The polarization of a cell based on its charge densities is given by the equation [2]:

$$P \equiv \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4 + \rho_5} \quad (2.2)$$

where ρ_i is the charge density at site i within the cell. For example, if the excess electrons are completely on sites 1 and 3, the cell's polarization is +1. If the excess electrons are completely on sites 2 and 4, the cell's polarization is -1. The numbered cell layout can be seen in Fig.2.6 on page 14.

Now that the energies and polarizations for isolated cells can be calculated, the interactions between neighboring cells need to be explored. This requires the addition of an interaction term to the single-cell Hamiltonian to represent the inter-cellular electrostatic potential energy [2]:

$$\hat{H}_{inter}^{cell} = \hat{H}_1^{cell} = \sum_{i \in cell, \sigma} V_i^1 \hat{n}_{i,\sigma} \quad (2.3)$$

where the interaction term, V , is given in terms of charge density. V_i^m , the potential at site i in cell m due to all other cells k , can be found using the equation [2]:

$$V_i^m = \sum_{k \neq m, j} V_Q \frac{\rho_j^k - \tilde{\rho}}{|\bar{R}_{k,j} - \bar{R}_{m,i}|} \quad (2.4)$$

where $\tilde{\rho}$ is a positive charge that is placed within each of the quantum dots to counteract the large resulting negative charge from all the electrons within the system, ρ_j^k is the charge density at site j on cell k , and the denominator is the distance from the i^{th} site of cell m to the j^{th} site of cell k .

Now we can put both pieces together to create the total Hamiltonian associated to one cell:

$$\hat{H}^{cell} = \hat{H}_0^{cell} + \hat{H}_1^{cell}. \quad (2.5)$$

This equation can be used to calculate the exact two-particle eigenstates. For higher numbers of cells, the calculations become exponentially more complex. The inter-cellular Hartree approximation can be incorporated to greatly reduce the calculation time [1]. It is a self-consistent and iterative approximation that utilizes an initial guess polarization for all cells. The corresponding charge densities are calculated based on the initial guess polarizations. A new polarization is calculated based upon interactions of the charge densities calculated in the previous step. The new polarizations are used in place of the initial guess polarization and the process is repeated until a convergence of the array is reached [1].

2.4. Thermal Study

The main operational fault of concern in QCA is temperature. Most theoretical studies have been performed at 0 K, but to become a feasible computational system, it has to work at much higher temperatures.

To simulate the effects of temperature in QCA, the thermal average of charge densities in each cell needs to be calculated. The thermal average of charge densities within a cell is given by [6, 8, 10, 13]:

$$\langle \rho_i \rangle = \frac{\sum_{n=1}^N \rho_{n,i} e^{-E_n / K_B T}}{\sum_{n=1}^N e^{-E_n / K_B T}} \quad (2.6)$$

where i is a site within the cell, K_B is the Boltzmann constant, E_n is the eigenenergy for energy level n , N is the total number of energy levels, and $\rho_{n,i}$ is calculated by using all the eigenstates for the ground state. The results from Equation (2.6) can then be plugged back into Equation (2.2) to obtain the cell polarization. This updated charge configuration is calculated through the canonical ensemble averages instead of the ground state quantum averages used when simulating at absolute zero (T_0). [6]

2.5. Cell-Cell Response

For QCA to function properly, the individual cells need to be easily influenced by the polarization of a neighboring cell. The response of one cell placed in close proximity to another cell is discussed in this section.

The cell spacing used in the simulation is 60 nm from center to center, and the temperature is set to 0 K. By simulating this most basic device, the target cell shows a strong response to a change in polarization of the driver cell as seen in Fig.2.2 [2]. The polarization on the plot ranges from -1 to 1, which can be replaced with binary 0 and 1 respectively [2].

With this strong cell to cell response, a signal can be transmitted from one cell to the next if placed in close proximity. Additional cells can be added in a row to form a binary wire, which will be discussed in Chapter 3.

The ability to transmit a signal with a perfect system is a great accomplishment, but to be a practical computational system, defects are a reality that will have to be explored.

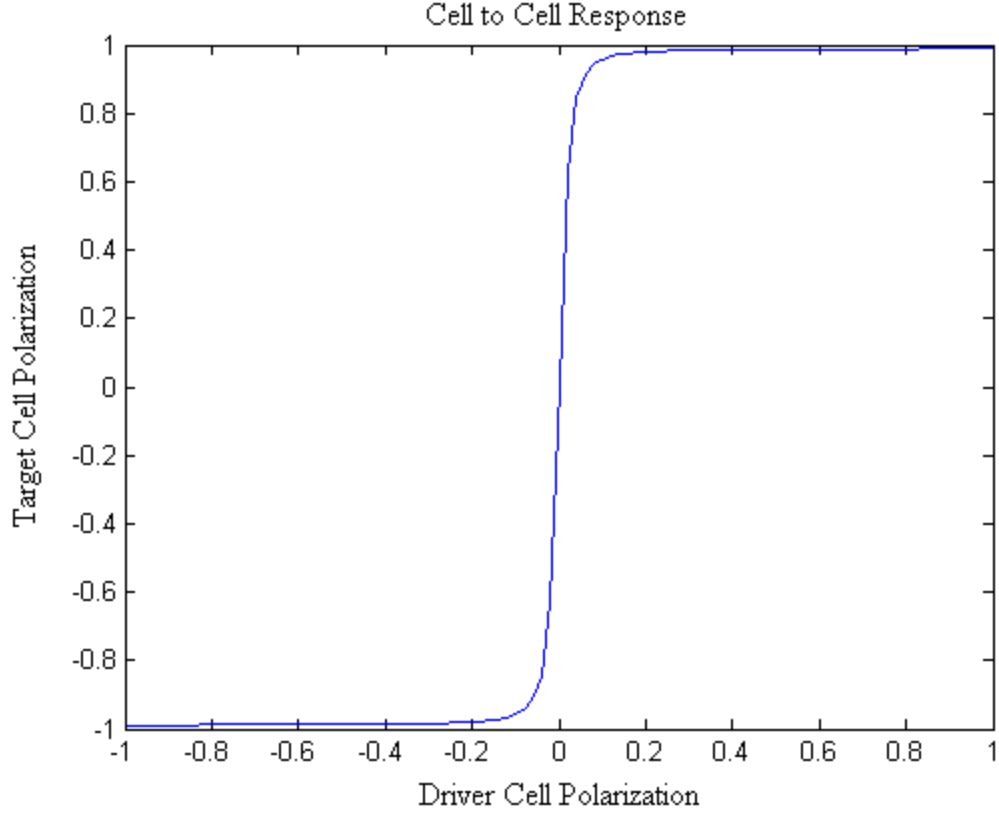


Figure 2.2: The cell-cell response curve of two neighboring QCA cells. [2]

2.6. QCA Defect Study

Defects and faults in any device can occur in various ways and forms depending on the device system (metallic, semiconductor, molecular, etc), design, manufacturing and fabrication technique and the operational environment. The QCA model under investigation in the present research project is designed for semiconductor materials. The defects in QCA can occur in several forms. The manufacturing defects can occur on the device level, or on the individual cell level. On the device level, a cell in an array could be displaced, rotated, or missing. Examples of these defects are depicted in Fig.2.3.

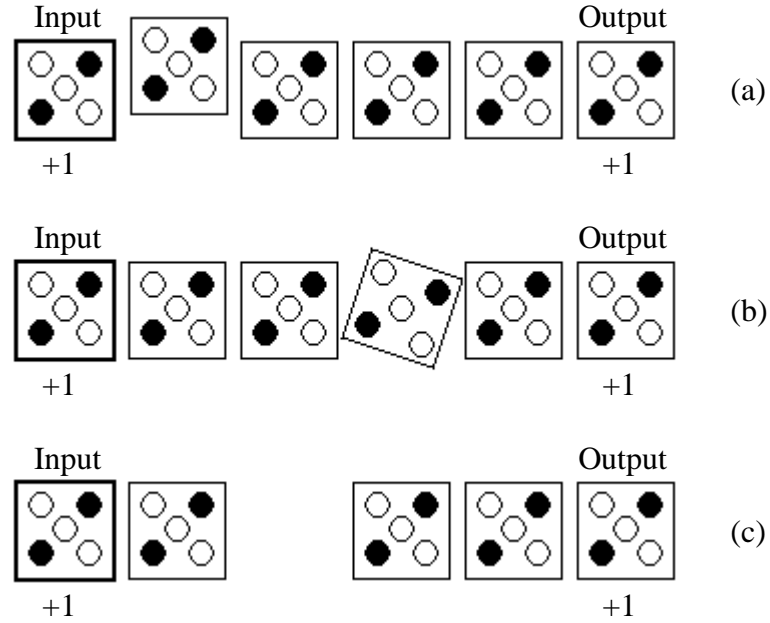


Figure 2.3: Device defects for a QCA binary wire: (a) displaced cell, (b) rotated cell, and (c) missing cell. [5, 7]

On the cell level, dots could be displaced from their ideal positions, distorted in size, the entire cell could be distorted in size, or a dot could be missing. Examples of these defects are shown in Fig.2.4.

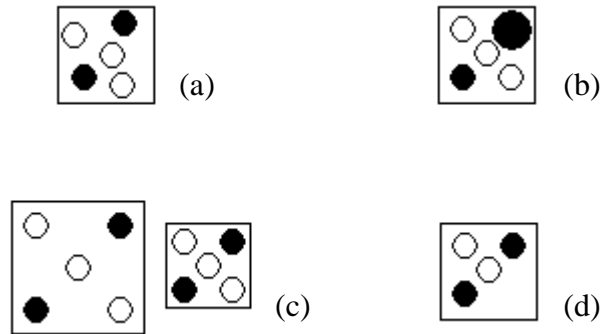


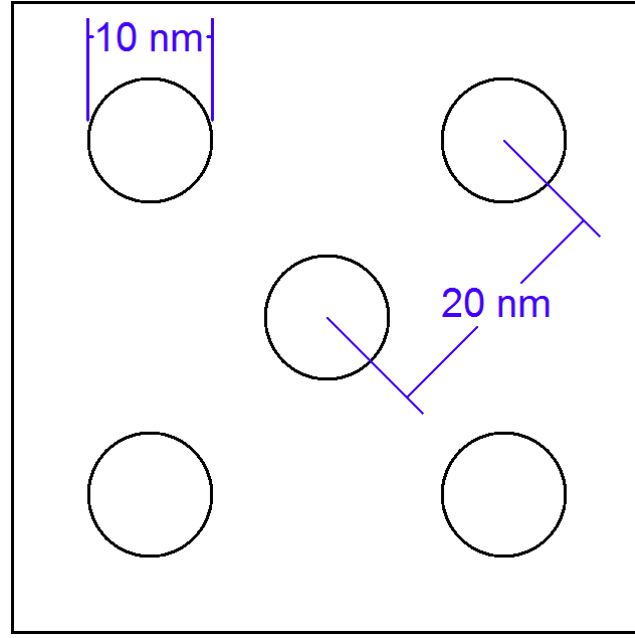
Figure 2.4: Cell level defects: (a) displaced dots, (b) distorted dot size, (c) distorted cell size, and (d) missing dot. [5, 7]

The operational defects include anything caused by the surrounding environment, such as temperature, stray charge, vibrations, etc. The main operational defect of concern for QCA is temperature. The current QCA model is only stable within a few degrees of absolute zero. Since very low temperatures are impractical and difficult to obtain, any increase in operational temperatures would be valuable.

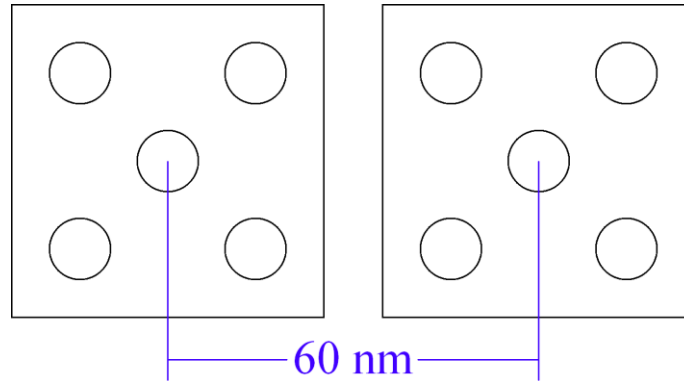
The defects of focus for the present thesis work are dot displacement and temperature effects.

2.7. QCA Defect Simulation Parameters

All devices simulated are comprised of five-dot cells since they have a better cell to cell response as compared to a four-dot cell [5-7]. Each dot is 10 nm in diameter, and the distance between the central dot to the corner dots is 20 nm for an ideal system as shown in Fig.2.5(a). The distance between central dot of one cell to the central dot of the next cell is set to 60 nm as shown in Fig.2.5(b). In other words the distance between neighboring cells is 60 nm. [1]



(a)



(b)

Figure 2.5: 5-dot cell layout with (a) dot dimensions and (b) cell spacing.

The displacement of dots is simulated using a uniform random distribution to allow the dots to be displaced in any direction from their ideal location, but limited so as to not overlap neighboring dots. A normal distribution might have been a better choice, but a uniform random distribution was used for comparison with previous simulations [6]. The displaced locations of dots are obtained using the following mathematical model introduced by T. Barclay [5]. The coordinates of dots are shown in Fig.2.6

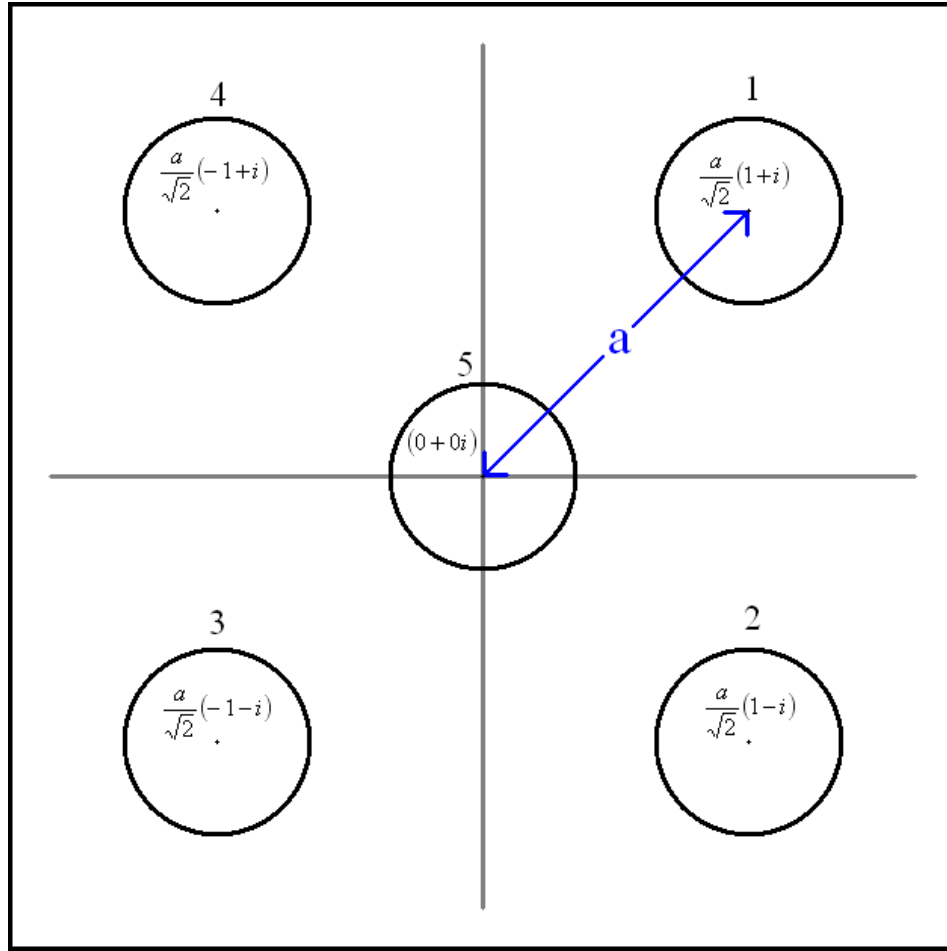


Figure 2.6: Design of a basic five-dot cell. [5]

and the displaced coordinates of dots 1 and 5 are given by:

$$x_1 = [1 + \sigma(rand(1) - 0.5)] \frac{a}{\sqrt{2}} \quad y_1 = [1 + \sigma(rand(1) - 0.5)] \frac{a}{\sqrt{2}} \quad (2.7)$$

$$x_5 = \sigma[rand(1) - 0.5] \frac{a}{\sqrt{2}} \quad y_5 = \sigma[rand(1) - 0.5] \frac{a}{\sqrt{2}} \quad (2.8)$$

where $rand(1)$ is a uniform random distribution number between 0 and 1, a is the distance between the two dots as shown in Fig.2.6, and σ is the displacement factor (DF). To avoid overlapping of dots, the equation

$$\sqrt{(x_1 - x_5)^2 + (y_1 - y_5)^2} \geq 2r \quad (2.9)$$

must be obeyed. By substituting (2.7) and (2.8) into (2.9) one finds the limit of σ to be:

$$(1 - \sigma)a \geq 2r; \text{ where } a = 4r \text{ and } 1 - \sigma \geq \frac{1}{2} \rightarrow \sigma \leq \frac{1}{2}. \quad (2.10)$$

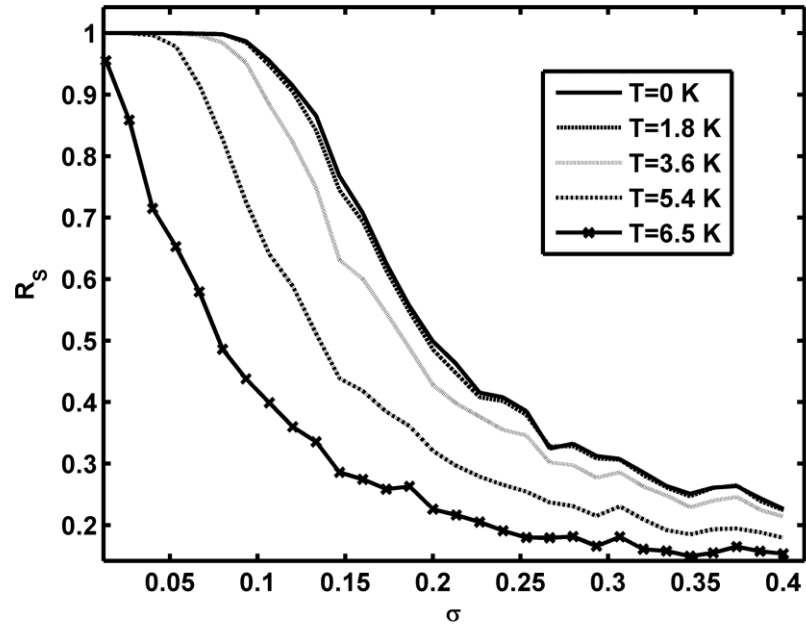
The limit of a dot displacement is obtained after some algebraic manipulation, which is found to be bounded between 0 and 0.5 [5]. It should also be mentioned here that a double-well potential barrier model was used to calculate the tunneling energy for different dot positions. M. Hendrichsen originally introduced and analyzed the model for finding the tunneling energy for different inter-dot distances [7]. Both models introduced in references [5] and [7] will be used in all simulations in the present thesis work.

Each basic device has been simulated at various temperatures. Graphs have been produced to show the success rate as a function of the displacement factor for each temperature. The success rate is defined as the total number of successful outputs divided by the total number of trials simulated, where a polarization greater or equal to 0.5 is counted as a success [5, 14]. The breakdown displacement factors (BDF) versus temperature effect have also been plotted. The BDF is the displacement factor (the parameter that determines the dot displacement) at which the device breaks down or fails to operate properly. The device is only considered successful if it produces the correct output one hundred percent of the times simulated, so the BDF is the highest displacement factor at which the success rate is 1.

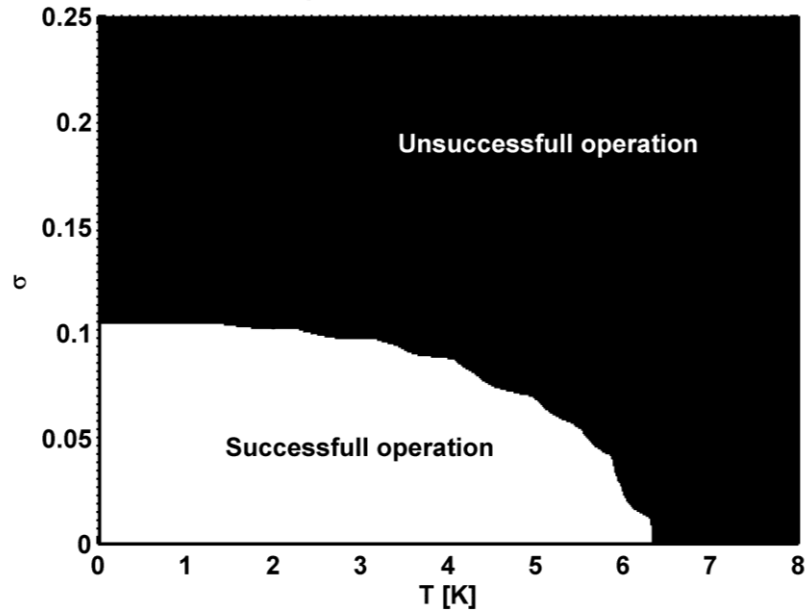
The number of trials used to simulate most of the devices is 7,000 per displacement factor for good statistical accuracy. The number of displacement factors used is 100 for most of the basic devices. Some more complex devices are tested at 2,000 trials, or 50 displacement factors to conserve resources. To improve computation speed, the inter-cellular Hartree approximation (ICHA) is used as mentioned above. The limitation tolerance is set to 0.00001 to find a global convergence for all cells in the device.

2.8. Previous Results

Some fault tolerances of QCA have been investigated prior to the current thesis work [3-5, 7, 14, 16]. Recently, some have focused on various fault tolerances of the most basic device: the binary wire [5, 7, 14, 16]. These results were produced from simulating a row of nine 4-dot QCA cells with a cell to cell spacing of 42 nm instead of the 5-dot system's 60 nm. The plots in Fig.2.7 show the simulation results for a binary wire in which the dots within each cell (excluding the input and output cells) are displaced about their ideal positions as seen in Fig.2.4(a). Fig.2.7(a) shows the success rate (R_S) versus the dot displacement factor (σ) for various temperatures. Fig.2.7(b) shows the phase diagram for the successful operation in the plane of temperature and dot displacement factor.



(a)



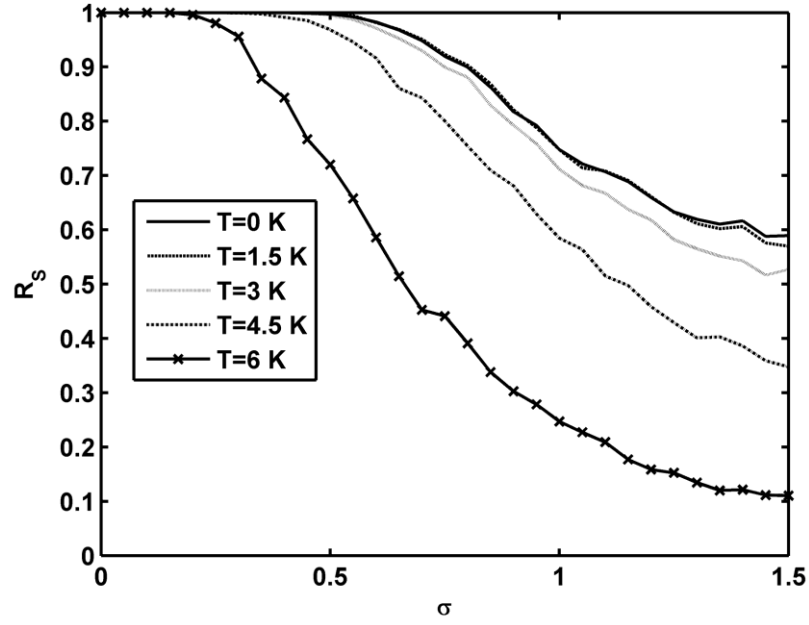
(b)

Figure 2.7: Simulation results for a 4-dot cell binary wire with displaced dots: (a) success rate versus dot displacement factor for various temperatures, and (b) phase diagram of the successful operation in the plane of temperature and dot displacement factor. [14]

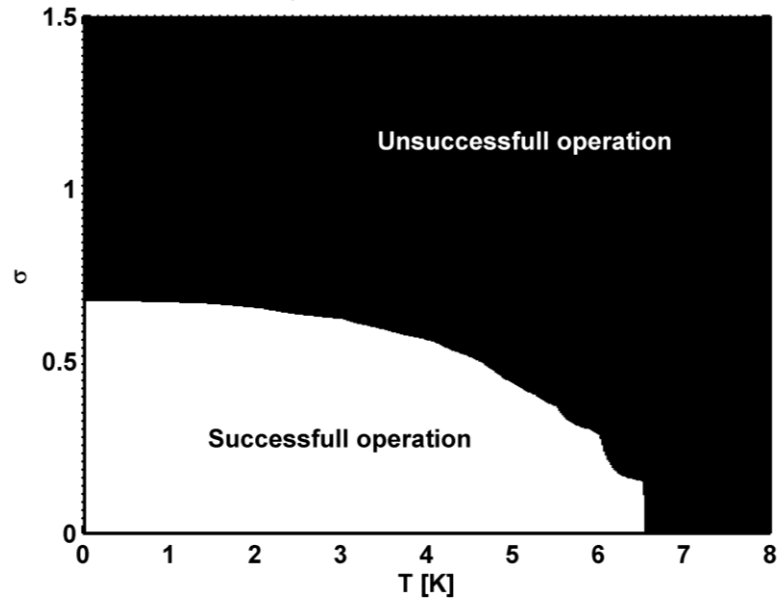
The results show a strong relationship between functionality and both dot displacement and temperature. The highest dot displacement factor the binary wire can have while still being stable is about 0.07. At 6.5 K, the wire is not even stable with all dots in their ideal locations. The wire shows little temperature dependence between 0 and 1.8 K. This would indicate that a binary wire could operate approximately unaltered if the temperature was to fluctuate ± 0.9 degrees from 0.9 K. If the dot displacement factor were restricted to within 0.8, the wire should be stable up to 5.4 K. This temperature can be reached with liquid Helium.

Another fault tolerance explored is the displacement of entire cells within the binary wire, as depicted in Fig.2.3(a). For this fault simulation, the cells are vertically displaced from their ideal positions using a normal distribution. The success rate versus the cell displacement factor is plotted for various temperatures in Fig.2.8(a). Here, the cell displacement factor range is greater than for dot displacement factor. This is due to QCA being more sensitive to cell level defects than array level defects. The success phase diagram is shown in Fig.2.8(b).

These results again show a strong correlation between success rate and both cell displacement and temperature. The operation is successful for low temperatures and smaller values of cell displacement, which is very similar to the dot displacement results mentioned above.



(a)



(b)

Figure 2.8: Simulation results for a 4-dot cell binary wire with vertically displaced cells: (a) success rate versus cell displacement factor for various temperatures, and (b) phase diagram of the successful operation in the plane of temperature and cell displacement factor.

Both dot displacement and cell displacement results show considerable temperature dependence. For temperatures above 6.5 K, the binary wire is unstable even under the ideal condition of no displacement. [14]

Missing dots is another fault that may occur in a QCA system. For this fault tolerance study, a given number of dots are removed from the cells in a random method. The success rate versus temperature is plotted in Fig.2.9 for various numbers of missing dots.

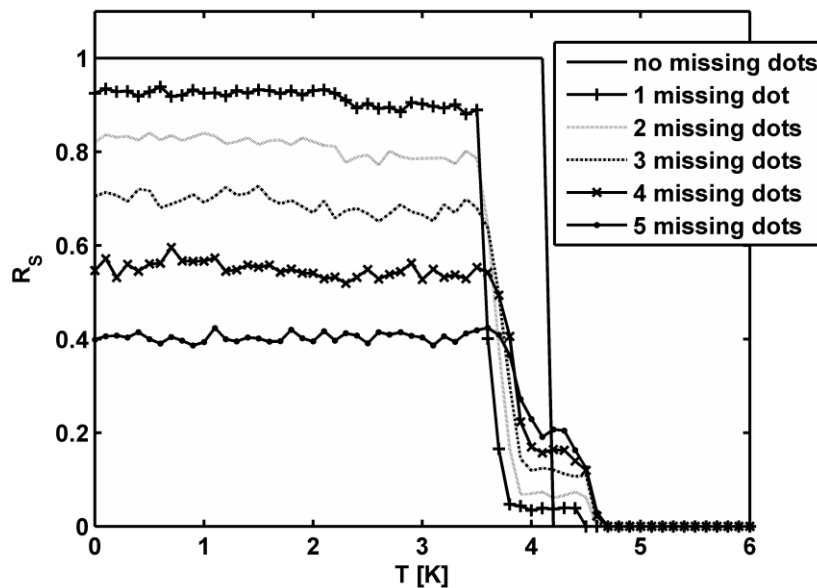


Figure 2.9: Success rate versus temperature for a binary wire with differing numbers of missing dots.

The results for missing dots in Fig.2.9 are compared to the ideal case of no missing dots. Even with only one missing dot, the device is unstable. This poor result could be greatly improved by using multiple lines of cells to make a multi-strand binary wire. The multi-strand binary wire could not be tested due to the limitations of the ICHA. One interesting result this data shows is that the device is nearly uninfluenced by

temperatures below 3.4 K. For higher temperatures, the success rate drops rapidly for any number of missing dots. These breakdown values are close to the critical temperature of 3.36 K corresponding to the tunneling energy between dots. [14]

These QCA fault tolerances are all for a 4-dot system, and limited to only one device. Additional devices are explored in the current thesis work using a 5-dot system to test the dot displacement and temperature dependence.

CHAPTER 3: BASIC LOGIC GATES

3.1. Introduction

Simple QCA devices have been successfully simulated and tested. The basic devices tested are a binary wire, inverter chain, inverter, majority gate (both AND and OR gates), and a crossover. Many of these devices have previously been tested by G. Anduwan and others [6, 14]. In the present thesis work, these devices and a few new devices were simulated using larger numbers of trials and more displacement factors to obtain a clear picture of the device functionality. For example, in the previous study by Anduwan [6], only 20 defect parameters were used whereas in this investigation the number is extended to 100. Also, the number of simulation trials has been increased to 7000 in almost all cases; in the past study, the maximum number of trials used was 2000. This allows for more detailed analysis and reduced statistical error. The device success rates show a strong correlation to dot displacement fault and to operation temperatures. The success rate versus dot displacement plots show distinct properties due to the dot displacement and temperature effects. Each device shows a decrease in success as either the dots are displaced, or as the temperature is increased. The basic QCA devices are discussed in further detail below with graphical layouts and plots of the simulated data.

3.2. Binary Wire

A binary wire can be constructed by placing QCA cells in a row as shown in Fig.3.1(a) [1]. The first cell is the driver cell or input cell which receives the initial polarization, the last cell is the output cell which all data is recorded from, and the 7 cells between the two are the target cells which are under the influence of dot displacement. Each target cell will receive information from the neighboring cell to the left, and pass it on to the next neighboring cell to the right. Although the function is simple, this is one of the most vital devices for QCA circuitry.

Fig.3.1(b) shows the success rate for the binary wire at six different temperatures ($T = 0, 1, 2, 3, 4,$ and 5 K) under the influence of dot displacement fault. The success rate is defined as the ratio of successful outputs divided by the total number of trials. A successful output is defined as the polarization of the output cell being greater than or equal to 50 % of the driver cell polarization. For the case of the binary wire, 2000 trials were used for each of the 101 equally spaced displacement factors. It is clearly shown that the success rate drops as the displacement factor is increased. It is also easy to see the success rate decreases as the temperature is increased. The thermal energy is responsible for the electrons tunneling in the dots and hence reduces the polarization value of the cells. Note the curves representing each temperature are not evenly spaced on the plot, even though each curve has a one degree difference from its neighboring curve.

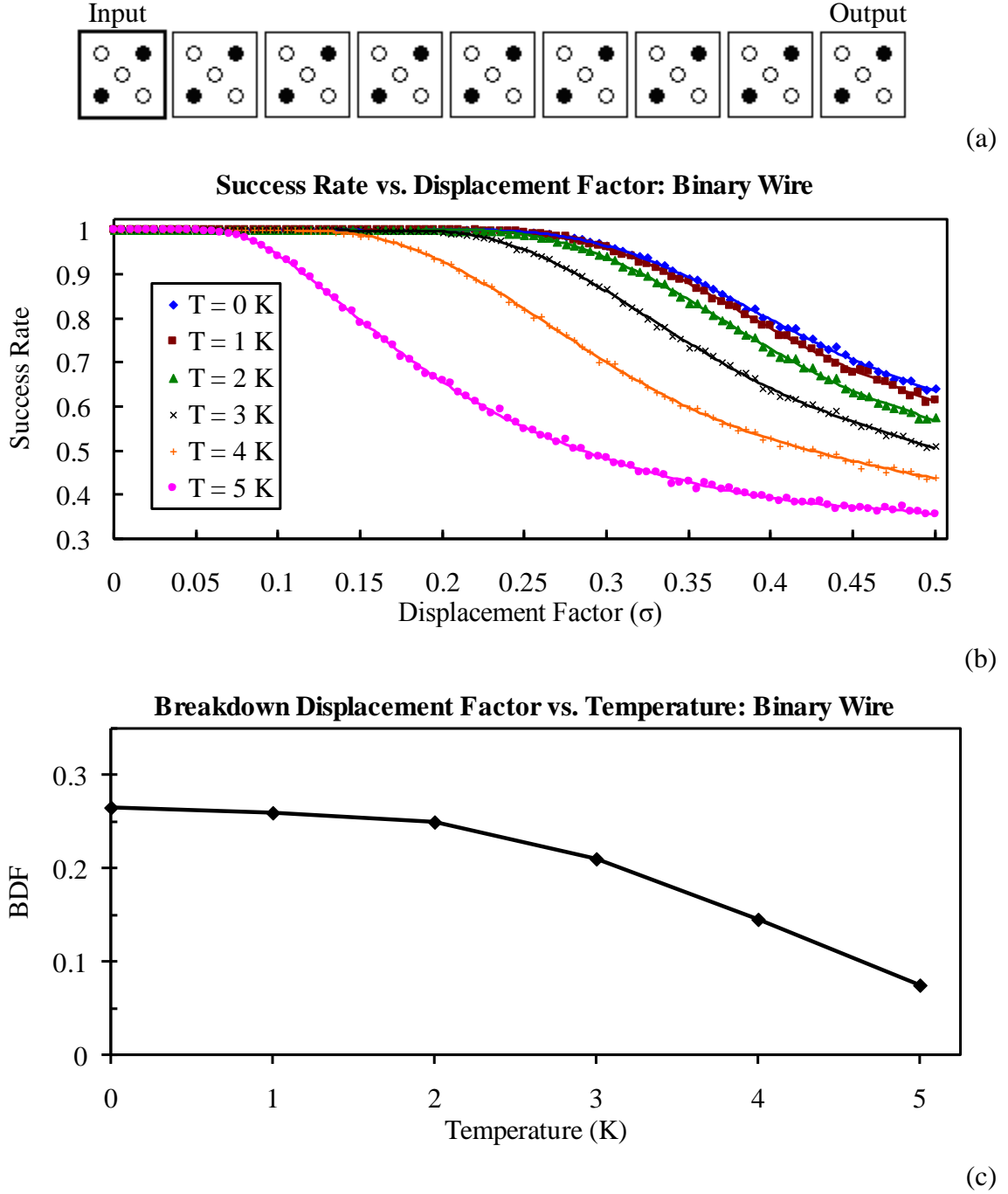


Figure 3.1: The simulation results for a 9-cell binary wire: (a) The cell layout with input of 1, (b) Success Rate versus Displacement Factor and (c) Breakdown Displacement Factor versus Temperature.

Fig.3.1(c) clearly shows a decrease in success as the temperature increases by showing the displacement factor at which the binary wire breaks down for each temperature. The breakdown displacement factor is almost invariant between 0 and 2 K with a difference of only 0.015. From 2 to 5 K, each degree changes the breakdown displacement factor by at least 0.040. This means at temperatures above 2 K, the device is less resistant to large dot displacements. Above 6 K, thermal variations cause the device to fail before any dot displacement is added [6]. At $T = 0, 1, 2, 3, 4$ and 5 K, the binary wire breaks down at a displacement factor of 0.265, 0.260, 0.250, 0.210, 0.145, and 0.075 respectively.

The binary wire was tested by our group previously [6, 14], but results were greatly limited by computing power. The previous results used about one fifth the number of displacement factors. The current increased number creates much less statistical error and is more accurate than the results presented in reference [14].

3.3. Inverter Chain

An inverter chain is similar to a binary wire, but with each cell rotated by forty-five degrees as seen in Fig.3.2(a) [1]. This causes the cell to polarize vertically or horizontally instead of diagonally. Each cell will push the next neighboring cell to the opposite polarization, thus inverting the signal as it passes through each cell as shown in Fig.3.2(a). The length of the inverter chain is important since changing the length by one cell will invert the output. The input cell, target cells, and output cell are all in the same location as the above mentioned binary wire.

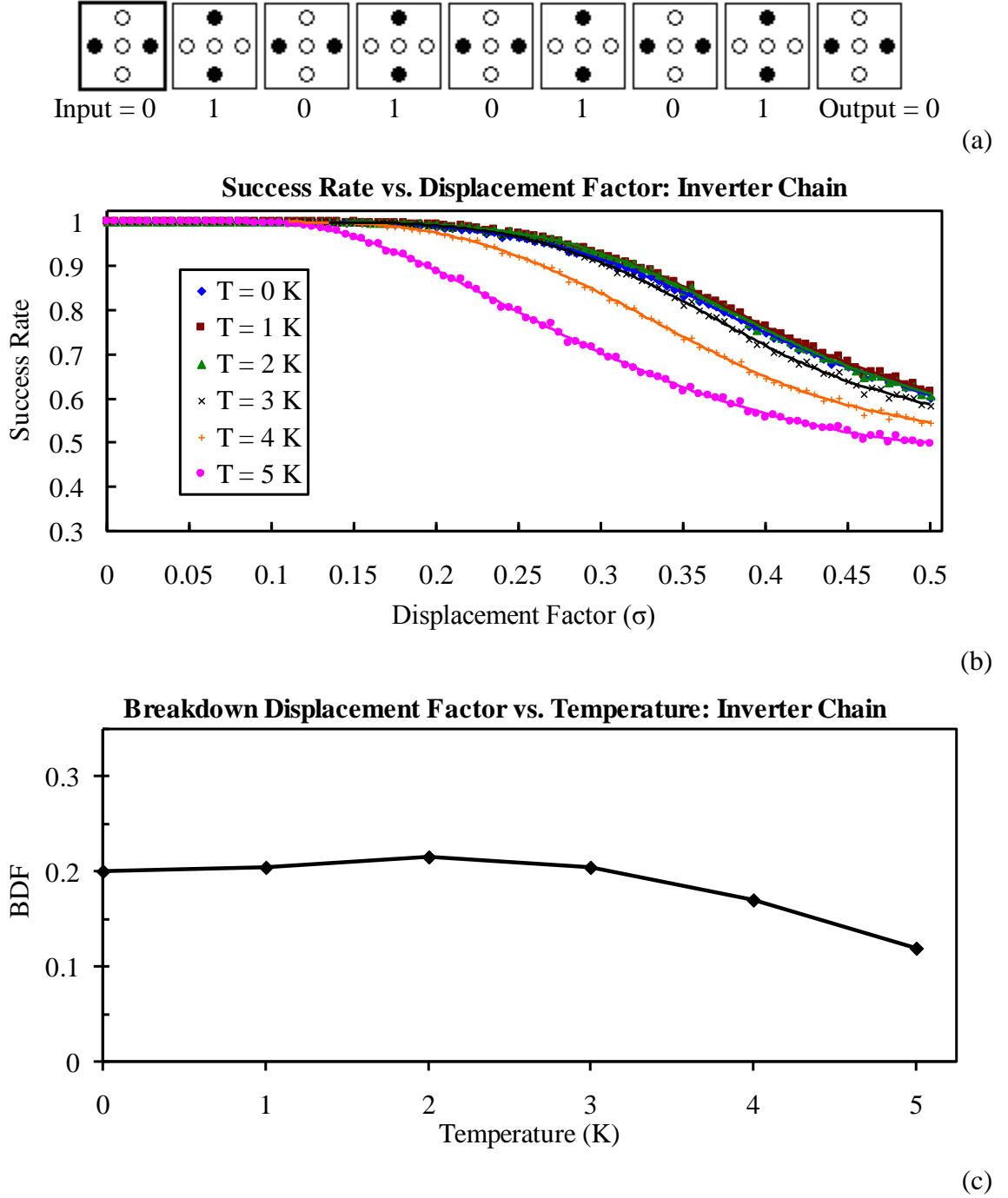


Figure 3.2: The simulation results for a 9-cell inverter chain: (a) The cell polarization layout for input of zero, (b) Success Rate versus Displacement Factor and (c) Breakdown Displacement Factor versus Temperature.

Fig.3.2(b) shows the success rate for the inverter chain at six different temperatures ($T = 0, 1, 2, 3, 4, 5$ K). It is shown that the success rate decreases as the temperature is increased. As seen with the binary wire, this is again due to thermal energy in the system causing the excess charges to become unstable. It is seen from Fig.3.2(b) that the device is almost invariant to temperature from 0 to 2 K. It is also easy to see the success rate drops as the displacement factor is increased.

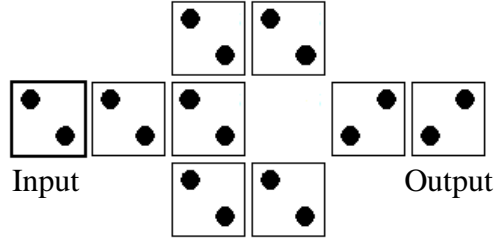
Fig.3.2(c) shows a decrease in success as the temperature increases. At $T = 0, 1, 2, 3, 4$ and 5 K, the inverter chain breaks down at a displacement factor of 0.200, 0.205, 0.215, 0.205, 0.170, and 0.120, respectively.

3.4. Inverter

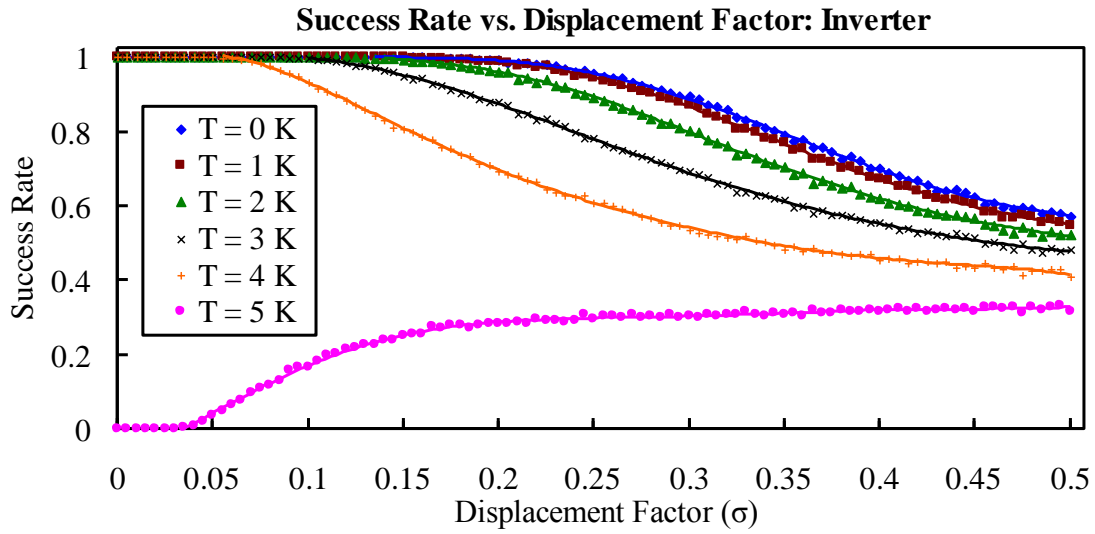
An inverter is a simple device that inverts an input signal. It behaves like the traditional Complementary Metal-Oxide-Semiconductor (CMOS) electronic device. An input of 1 will lead to an output of 0 and vice versa. There are several different designs to invert a signal in QCA, but two are more commonly used than the others. The first design tested splits the signal into two branches that influence another binary wire diagonally or offset as shown in Fig.3.3(a) [1]. This design will be addressed simply as an “inverter” from here on. The left-most cell is the driver, the right-most is the output cell, and the 7 cells between are the target cells.

Fig.3.3(b) shows the success rate for the inverter at five different temperatures ($T = 0$ to 5 K). It is shown that the success rate decreases as the temperature is increased for 0 to 5 K. It is also easy to see the success rate drops as the displacement factor is increased for 0 to 4 K. The 5 K curve for this device shows exceptionally unusual

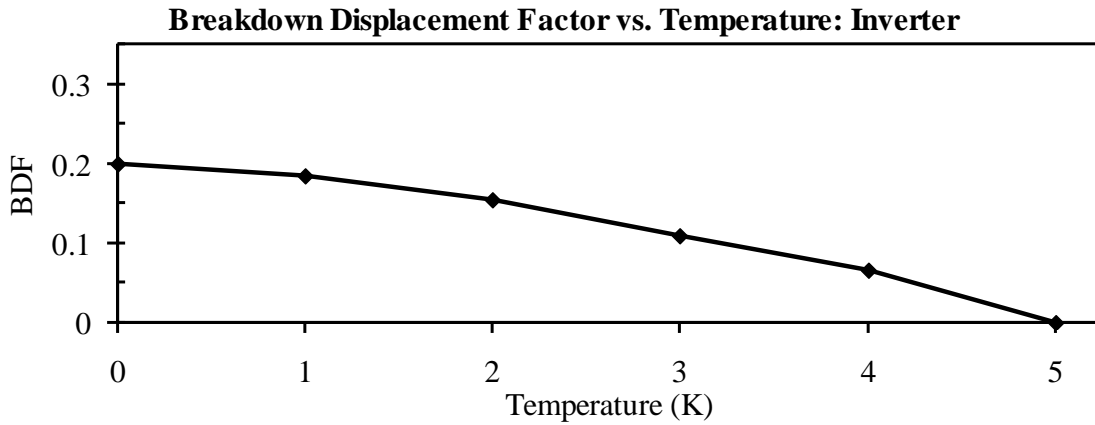
behavior. It appears to improve tolerance of dot displacement with the increased temperature. Upon review of previous results, the 5 K curve was not shown [6].



(a)



(b)



(c)

Figure 3.3: The simulation results for an inverter: (a) The cell layout, (b) Success Rate versus Displacement Factor (note the change in scale on the y-axis to show the full 5 K curve) and (c) Breakdown Displacement Factor versus Temperature.

Since the answer to the unusual behavior had not been solved, the program was run at various temperatures between 4 K and 5 K to determine what occurs in that small one degree region. These additional trials produced the results shown in Fig.3.4. It is clear that the device completely breaks down at temperatures higher than 4.6 K. Even with no defect, the inverter cannot produce a strong enough polarization to produce a valid output. This indicates a new QCA critical temperature between 4.6 K and 4.7 K, in which any increase will cause even a perfect device to fail. With this development, it is determined that the current QCA model cannot operate above this critical temperature. The higher temperature curves start with no successful outputs because the device is unable to produce a strong enough output polarization to be considered a binary 0 or 1, so the device fails every time.

All of the curves in Fig.3.4 tend to converge to a success rate of about 0.38 as displacement is increased, but this is merely due to random displacements giving the correct output by chance. In the range of cell polarization from -1 to +1, only 0.5 to 1 are counted as a success if the expected output is a binary 1. From pure randomness, there would be a 25 % chance of landing in the successful range, resulting in a success rate of 0.25. Factor in the QCA cell's natural bistable behavior, and the chances of landing in the successful range increase. From this theory, the 0.38 success rate convergence is no surprise.

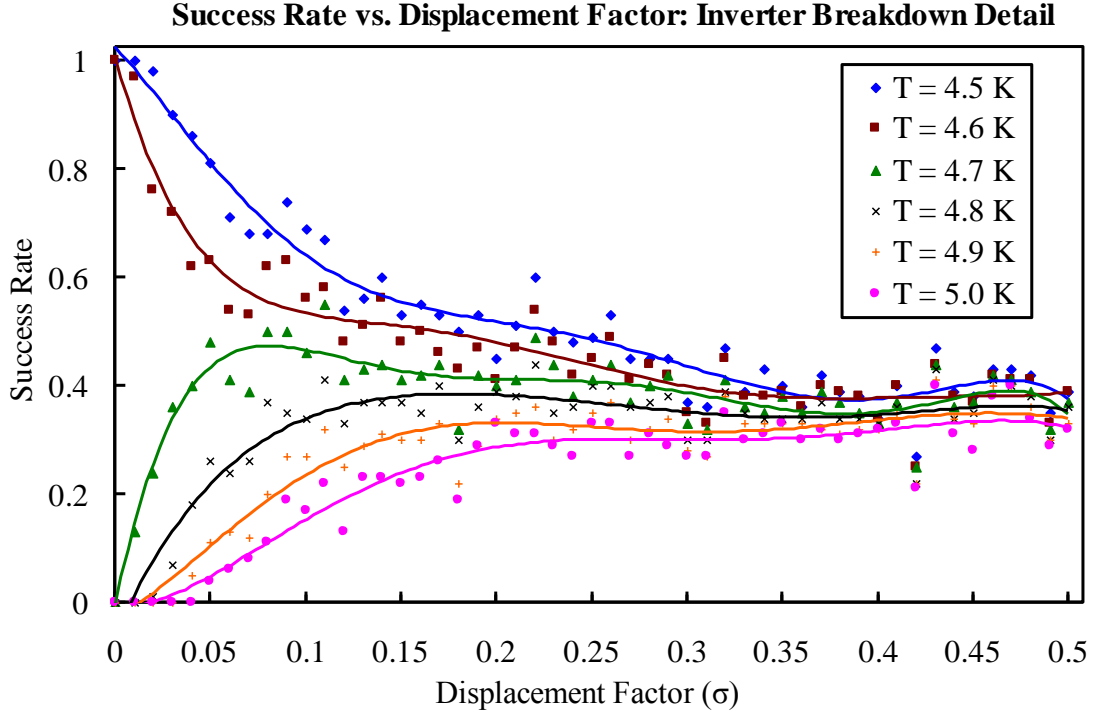
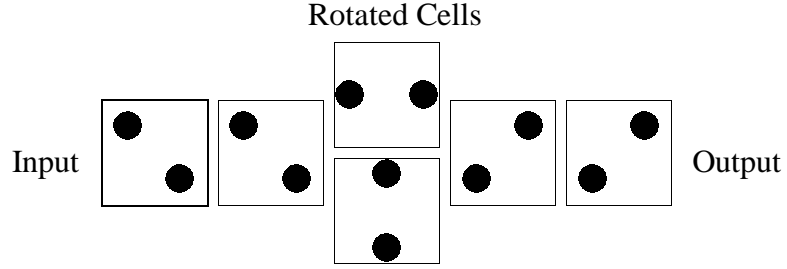


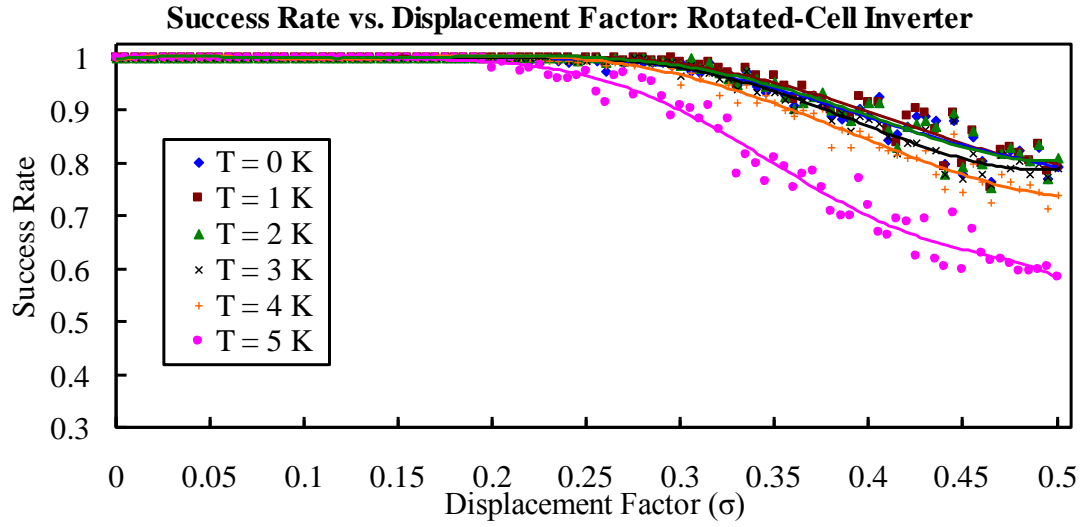
Figure 3.4: Success Rate versus Displacement Factor for an inverter between 4.5 and 5 K.

Fig.3.3(c) shows a decrease in success as the temperature increases. At $T = 0, 1, 2, 3, 4$ and 5 K, the inverter breaks down at a displacement factor of $\sigma = 0.200, 0.185, 0.155, 0.110, 0.065$, and 0.000 respectively. This indicates that even a perfect system at temperatures at or above 5 K will not function properly.

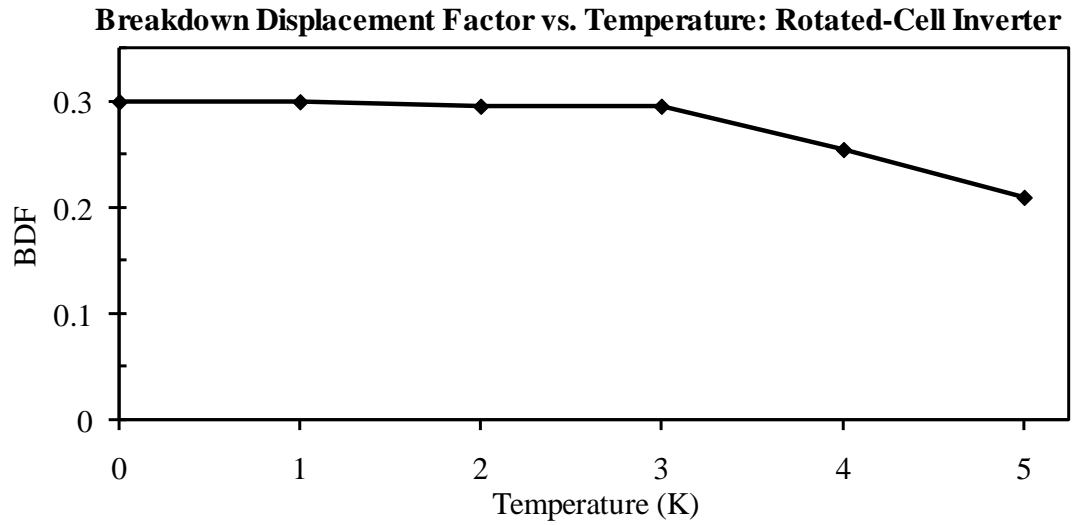
The above design for an inverter works well, but uses many cells for a simple operation. Another inverter design can be used which is comprised of removing one cell from a binary wire, and replacing the missing cell with two offset and rotated cells as shown in Fig.3.5(a) [17]. This design requires fewer cells, but adds the increased difficulty of creating rotated cells mixed with normal or perpendicular cells. The new design will be referred to as a “rotated-cell inverter” from here on. The simulation results for this device are entirely new.



(a)



(b)



(c)

Figure 3.5: The simulation results for rotated-cell inverter: (a) The cell layout, (b) Success Rate versus Displacement Factor and (c) Breakdown Displacement Factor versus Temperature.

In this particular device, a small number of trials (200) have been used to find out the general fault tolerant and thermal characteristics on the operation. The general trend of the operational (thermal) defect and the manufacturing or fabrication defect (displaced dots in the cells) is almost the same as the other devices discussed above. The rotated-cell inverter design performs better in the presence of defect and temperature than the inverter shown in Fig.3.3(a). The breakdown displacement factor (BDF) values at $T = 0, 1, 2, 3, 4$ and 5 K are 0.300, 0.305, 0.295, 0.300, 0.255 and 0.200 respectively. Notice that the BDF value for the inverter made from normal cells at 5 K is only 0.035 and that for the inverter made from the rotated cells is 0.2. Therefore, the rotated-cell inverter is much more tolerant to thermal as well as to the fabrication defects.

3.5. Majority Gate: AND/OR Gates

A majority gate is comprised of four cells surrounding a central cell. Three of the four surrounding cells act as inputs and the fourth one acts as an output. The central cell is influenced by the three inputs, and then its polarization is passed on to the output cell on the far right in Fig.3.6. Some fault tolerance study of majority gates have been previously published by G. Anduwan [6], but they are shown here in higher resolution and accompanied by extensive analysis.

An AND and an OR gate can be constructed from the majority gate by setting one permanent or fixed input value. The three inputs in the majority gate in Fig.3.6 are A, B and C. In this thesis work, the input C is considered to be the program line or the fixed input. An AND gate is constructed by permanently setting one of the inputs in a majority gate to a polarization of -1 to represent a binary 0 ($C = 0$). This will allow for an output

of 1 only if both of the other inputs are 1, just like its CMOS cousin. Similarly, the fixed input in an OR gate is 1 ($C = 1$), and the output of the majority gate will be 1 if at least one of the other two inputs is 1.

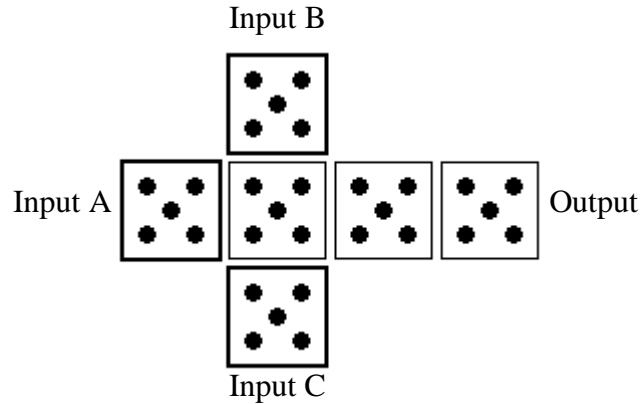


Figure 3.6: The unpolarized cell layout for a 3-input majority gate.

All possible combinations of inputs for an AND gate are $(ABC =)$: 000, 010, 100 and 110, and for an OR gate are $(ABC =)$: 001, 011, 101 and 111. A schematic representation of all possible configurations is shown in Fig.3.7. The different input configurations should be thought of as polarization states of the majority gate, rather than separate gates. The combinations of inputs in the AND 000 and the AND 100 are the same as the OR 111 and the OR 011 gates, respectively. The AND 010 and the OR 001 also have identical physical properties to the AND 110 and the OR 101, respectively. This may seem counterintuitive, but it is more transparent in Fig.3.7 that the matching gates have the same combinations of interfering inputs. Interference between neighboring cells is highlighted in blue, and interference between diagonal neighbors is highlighted in red. The influence of the electrostatic interactions on the central cell is the

same in all matching configurations shown with a connecting line. Preliminary investigations in the present work confirmed the above statement.

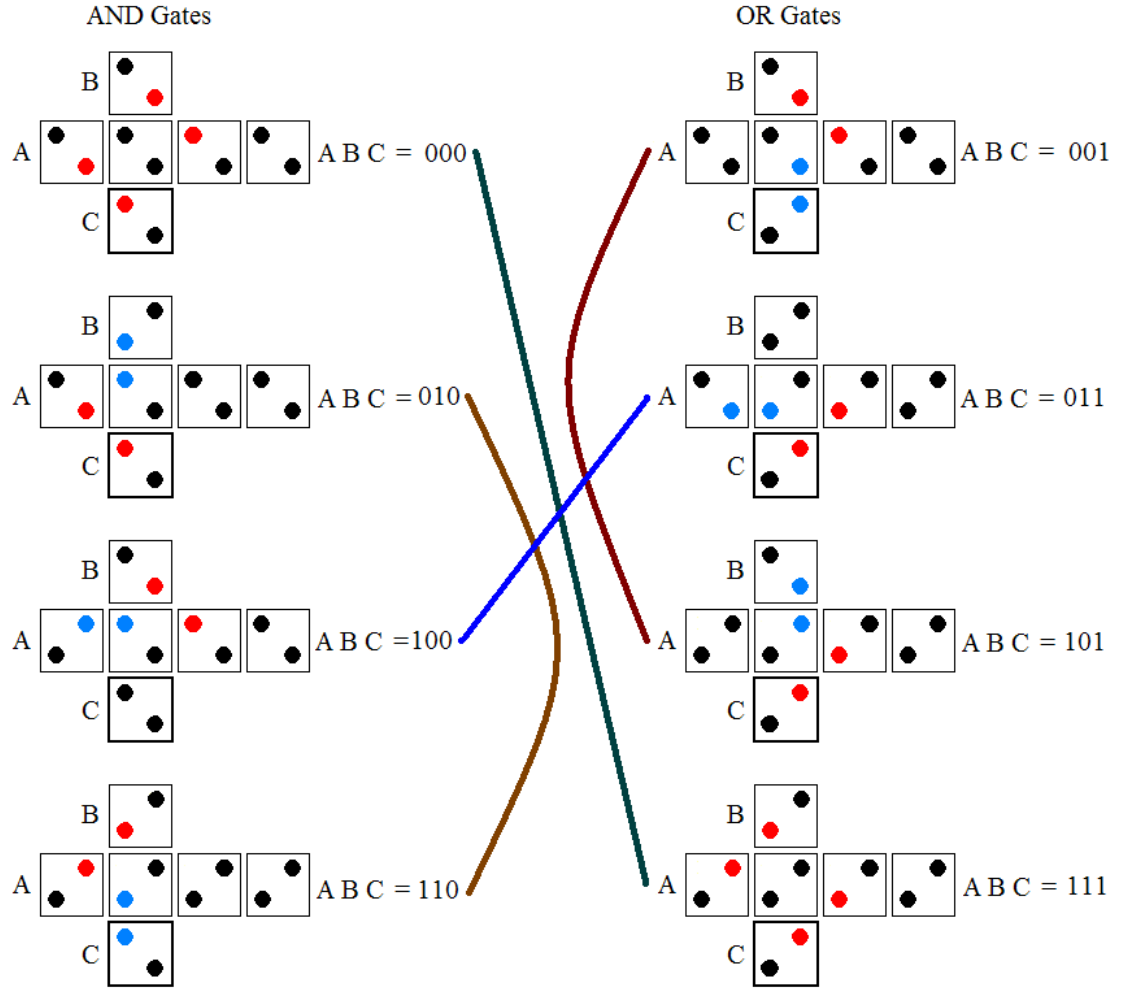


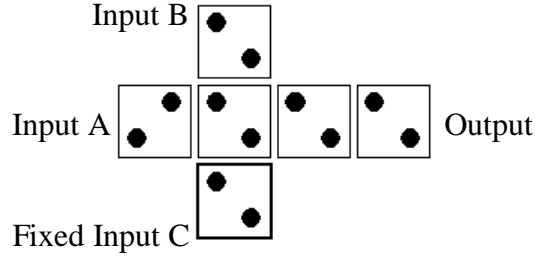
Figure 3.7: Visual connection of redundant majority gate inputs. The lines connect gates that will have the same success rates, but with opposite output values. Diagonal interfering inputs are colored in red and neighboring interfering inputs are labeled in blue.

3.5.1 AND Gate

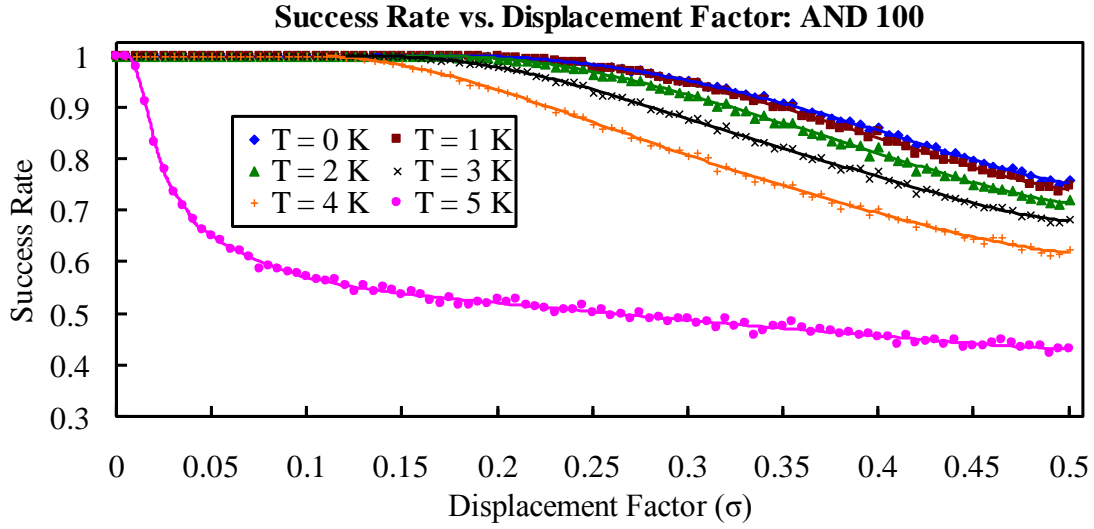
As mentioned above, an AND gate is constructed by permanently setting one of the inputs in a majority gate to 0. This will allow for an output of 1 only if both of the other inputs are 1. Results for the AND 100 and 110 gates are presented here.

The first AND gate tested is the AND 100. This is one of the more stable majority gates since none of the three inputs interfere with each other by having neighboring corner charges as seen in Fig.3.8(a). This is the only majority gate presented in the present thesis work that was not presented by G. Anduwan [6].

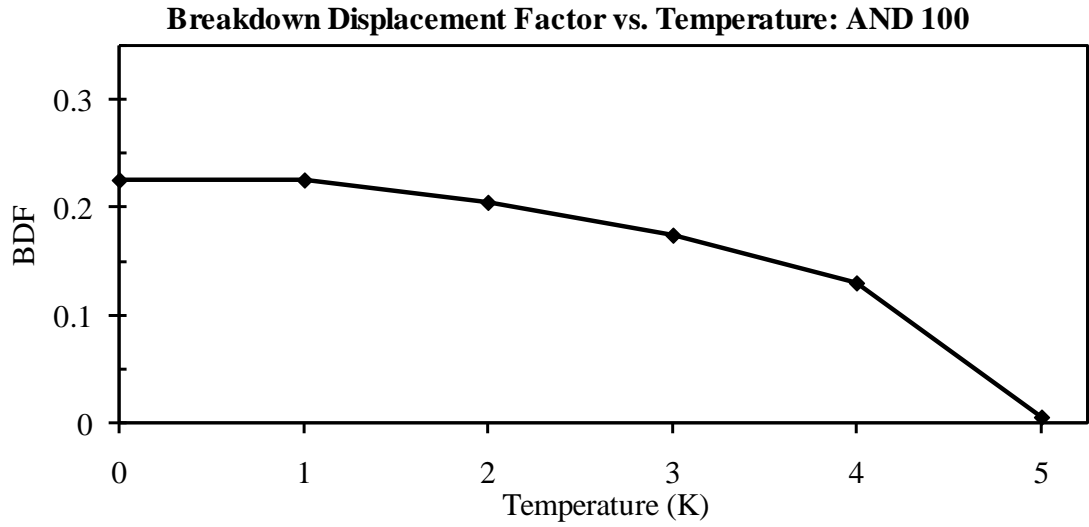
Fig.3.8(b) shows the success rate for the AND 100 gate at six different temperatures. It is clearly seen that the success rate decreases as the temperature is increased. It is also noticeable that the success rate drops as the displacement factor is increased. The curves clearly reflect the thermal tolerance at a specific defect parameter. For example, at $\sigma = 0.15$, the AND gate will operate properly close to 4 K temperature. The strange 5 K behavior is similar to the behavior of the inverter results shown in Fig.3.3(b) and Fig.3.4. To our knowledge, the fault tolerance of the AND 100 gate has not been investigated by any previous researchers, while the AND 110, OR 101, and OR 111 gates were investigated by Anduwan [6]. The drastic drop in success rate between the 4 K curve and the 5 K curve is due to the 5 K curve being near the critical temperature for the AND 100 gate. This is comparable to the critical temperature of 4.6 K stated in the inverter results discussion of section 3.4.



(a)



(b)



(c)

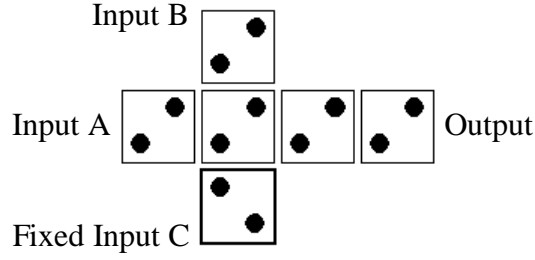
Figure 3.8: The simulation results for an AND gate ($ABC = 100$): (a) The cell layout, (b) Success Rate versus Displacement Factor and (c) Breakdown Displacement Factor versus Temperature.

Fig.3.8(c) shows a decrease in success of the device as the temperature increases. At $T = 0, 1, 2, 3, 4$ and 5 K, the AND 100 gate breaks down at a displacement factor of 0.225, 0.225, 0.205, 0.175, 0.130, and 0.005, respectively. The trend of the curve is smooth as expected; the breakdown displacement factor values decrease with the temperature.

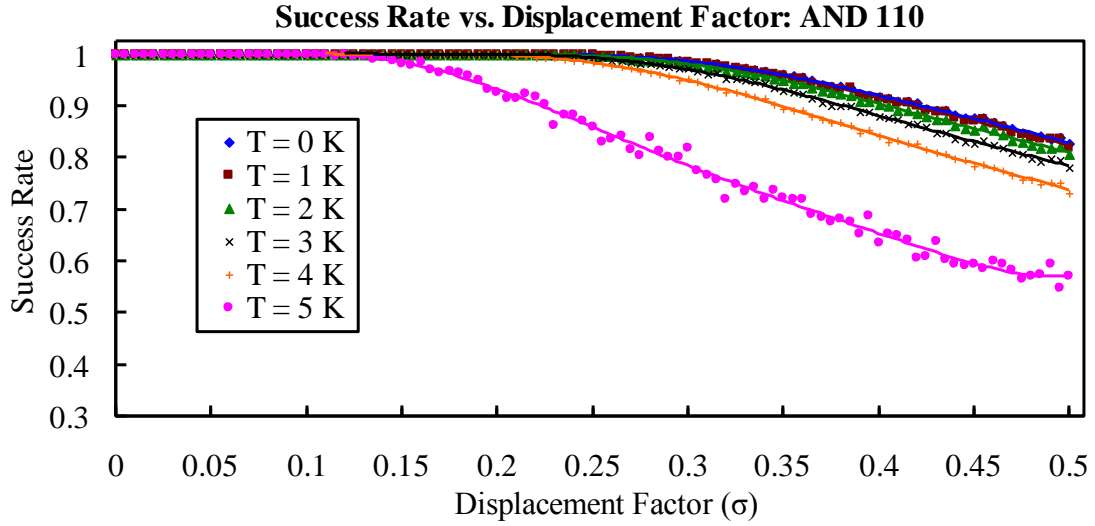
The second majority gate tested is the AND 110. The layout of the AND 110 gate is shown in Fig.3.9(a).

Fig.3.9(b) shows the success rate for the AND 110 gate at six different temperatures. It is clearly shown that the success rate decreases as the temperature is increased. It is also easy to see the success rate drops as the displacement factor is increased.

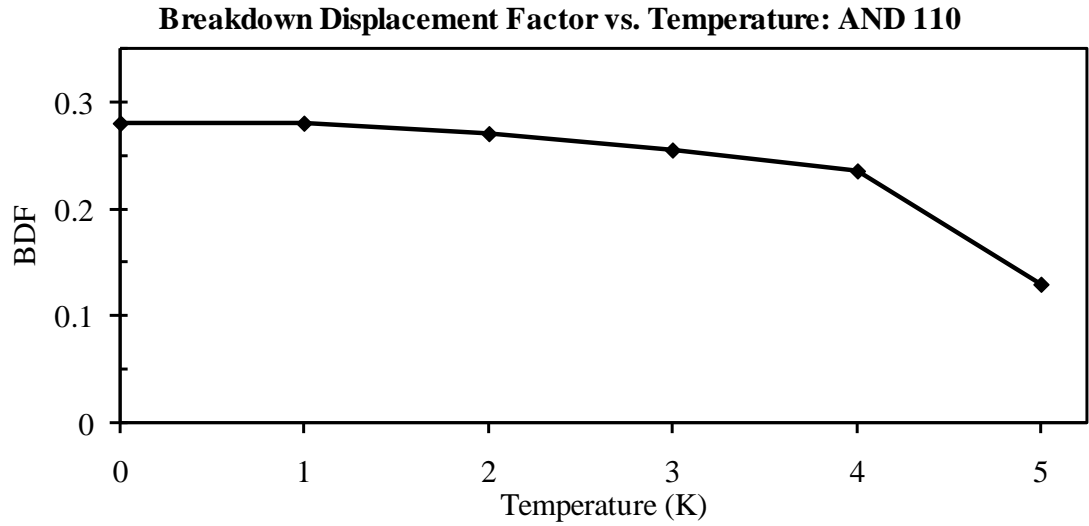
Fig.3.9(c) shows a decrease in success as the temperature increases. At 0, 1, 2, 3, 4 and 5 K, the AND 110 gate breaks down at a displacement factor of 0.280, 0.280, 0.270, 0.255, 0.235, and 0.130, respectively. It is noticeable that the breakdown displacement factors for the AND 110 input configuration in each temperature is higher than the AND 100 configuration. For comparison, the success rate versus displacement factor for the AND 100 and the AND 110 gates at 0 K are plotted in Fig.3.10.



(a)



(b)



(c)

Figure 3.9: The simulation results for an AND gate (ABC = 110): (a) The cell layout, (b) Success Rate versus Displacement Factor and (c) Breakdown Displacement Factor versus Temperature.

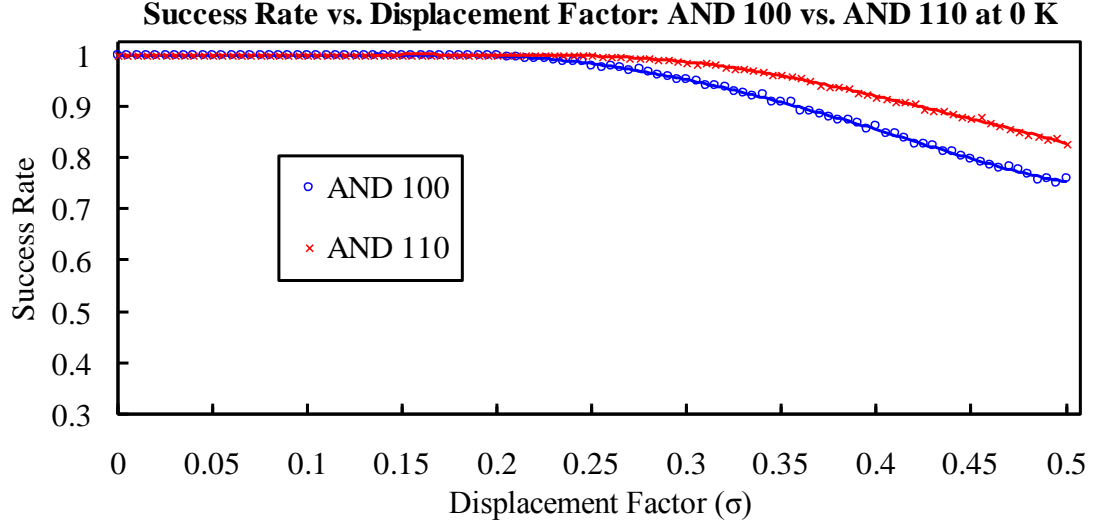


Figure 3.10: Comparison of Success Rate versus Displacement Factor for the AND 100 and the AND 110 gates at 0 K.

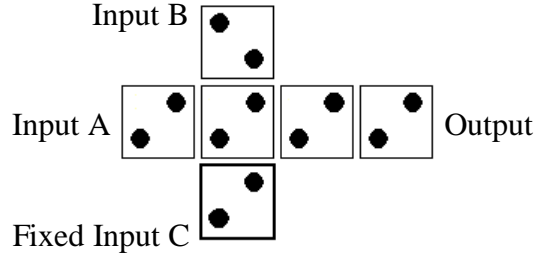
At absolute zero, the breakdown points are 0.22 and 0.28 for the AND 100 and the AND 110 inputs. In the case of the AND 110, the top and bottom inputs (B and C) contain opposite polarizations and have less influence on the polarization of the output cell (5th cell) which is to the right of the central device cell. For the AND 100 gate, the top and bottom inputs (B and C) are of the same polarization, and the excess charge on the bottom right corner dot in the input B negatively influences the charge polarization of the 5th cell as indicated by red color in Fig.3.7. Therefore, the AND 110 will permit a stronger charge polarization to be passed to the output cell and hence will function better.

3.5.2 OR Gate

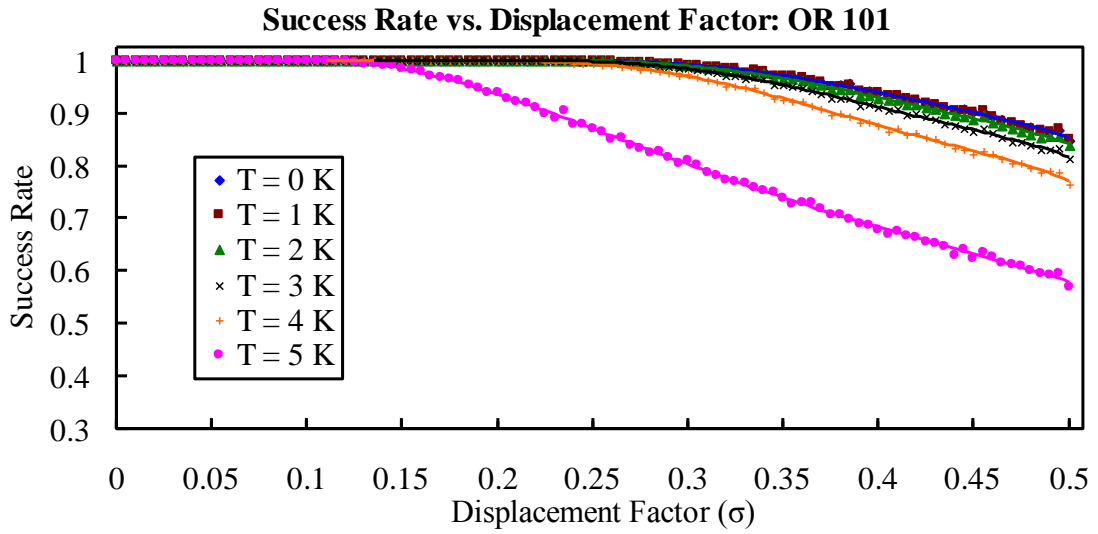
An OR gate is similar to an AND gate, but instead of permanently setting one input to 0, it will be set to 1. As mentioned above, this allows for an output of 1 if either or both of the other two inputs are 1. Here, the results for the OR 101 and the OR 111 will be discussed. A schematic representation of the OR 101 is shown in Fig.3.11(a).

Fig.3.11(b) shows the success rate for the OR 101 gate at six different temperatures, $T = 0, 1, 2, 3, 4$, and 5 K. Both the thermal and defect tolerance of the device is observed from the success rate versus displacement factor graphs shown in Fig.3.11(b). It is clearly seen that the success rate of the gate decreases as the temperature is increased. It is also easy to notice the success rate drops as the displacement factor is increased.

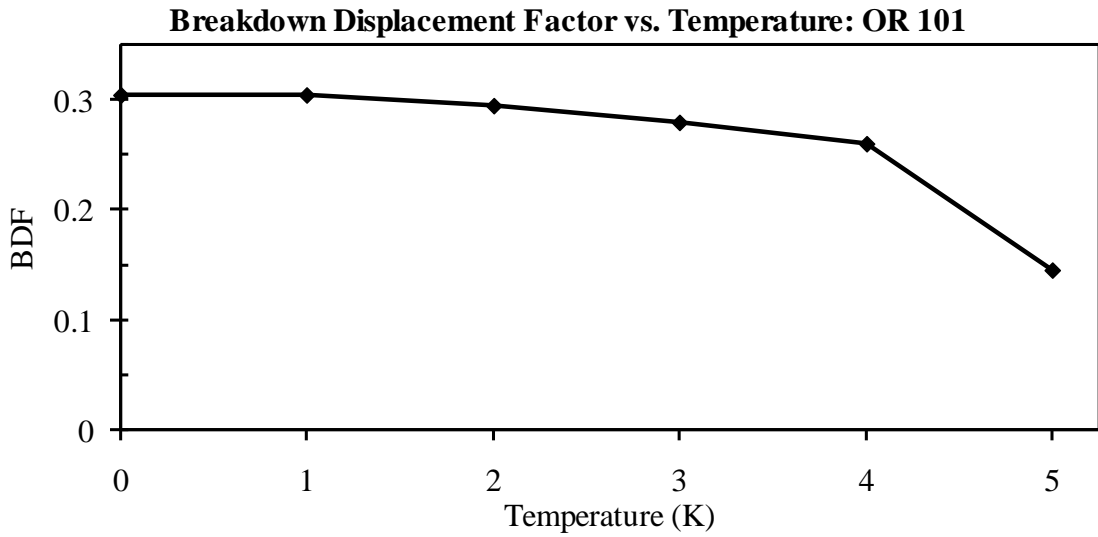
Fig.3.11(c) shows a decrease in success as the temperature increases. At $T = 0, 1, 2, 3, 4$ and 5 K, the OR 101 gate breaks down at a displacement factor of $\sigma = 0.305, 0.305, 0.295, 0.280, 0.260$, and 0.145 respectively. It is clearly observed that the functionality of the device monotonically decays with increased temperature.



(a)



(b)



(c)

Figure 3.11: The simulation results for an OR gate ($ABC = 101$): (a) The cell layout, (b) Success Rate versus Displacement Factor and (c) Breakdown Displacement Factor versus Temperature.

In the present study, it is also observed that although the OR 101 and the AND 110 are both majority gates with the same inputs of two 1's and a 0, the layout of the gate makes a difference in the success rate. The electrostatic interactions between the electrons on the corner dots in the input cells A and B in the AND 110 play a crucial role in the device operation. The two interfering input dots are marked with red color in Fig.3.12. In the AND 110 gate this effect is stronger on the device cell (the central cell) than in the OR 101 gate. Therefore, the OR 101 will be more stable and function better than the AND 110 gate.

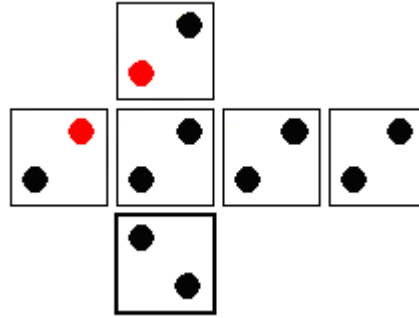


Figure 3.12: Interference between two inputs in AND 110 highlighted in red.

The OR 101 gate outperforms the AND 110 gate, which is easily seen in the comparison of the success rates at 0 K in Fig.3.13 shown below. At absolute zero temperature, the BDF values for the AND 110 and OR 101 are 0.28 and 0.30, respectively.

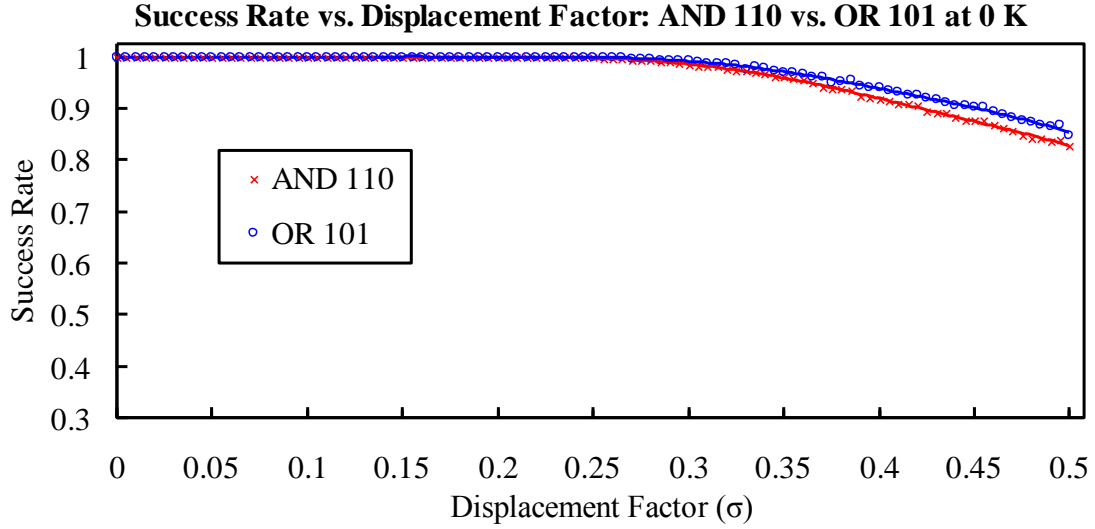
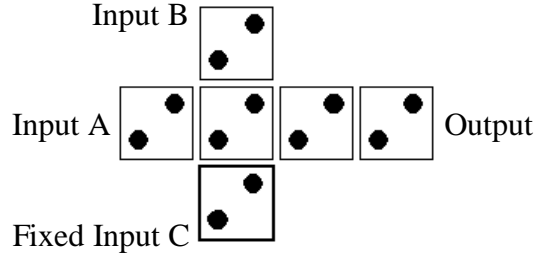
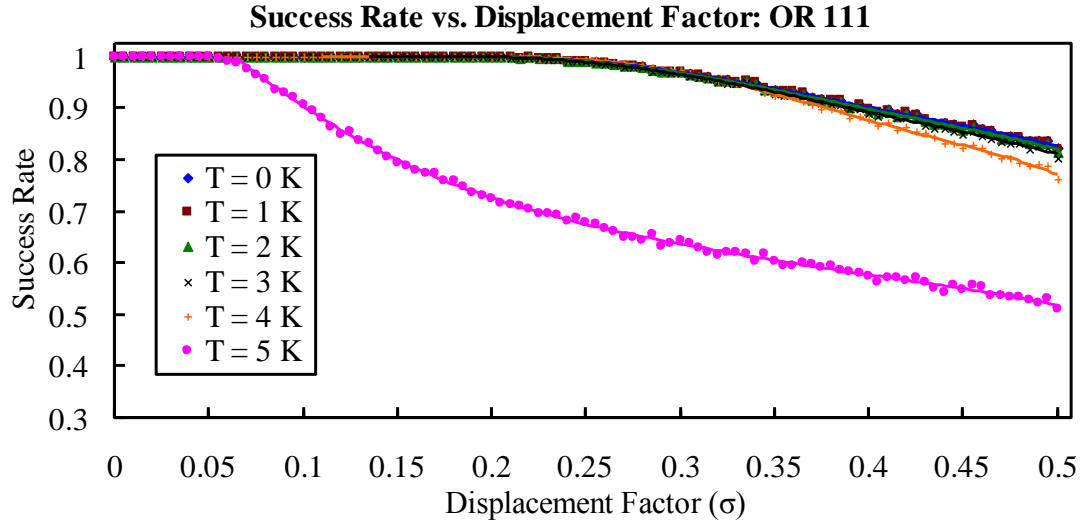


Figure 3.13: Comparison of the AND 110 and the OR 101 gates.

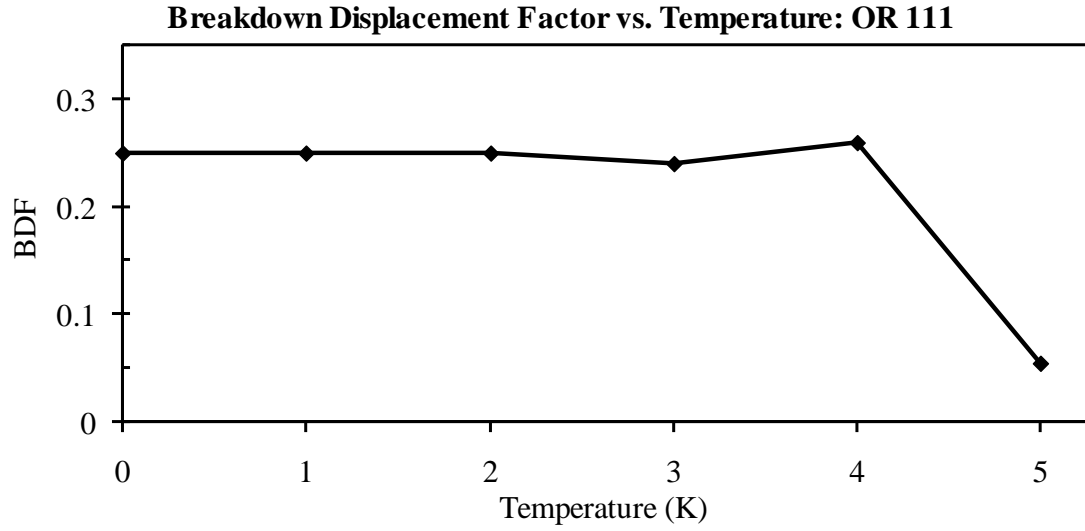
The last OR gate to explore is the OR 111, which can be seen below in Fig.3.14(a). All inputs are the same which intuitively would mean it should be the most stable configuration in the OR gate family. In real life that is not the case. Results show that it is less stable compared to the OR 101 gate. As discussed earlier for the AND 110 gate, the electron-electron interactions between the input cells A and B, and between the input cell C and the output cell (5th cell) will reduce the out going charge polarization in the device. These interfering charges are indicated by color in Fig.3.7. Therefore, the OR 111 gate will be less stable in the presence of defect and temperature compared to the AND 110 and the OR 101 gates.



(a)



(b)



(c)

Figure 3.14: The simulation results for an OR gate ($ABC = 111$): (a) The cell layout, (b) Success Rate versus Displacement Factor and (c) Breakdown Displacement Factor versus Temperature.

Fig.3.14(b) shows the success rate for the OR 111 gate at six different temperatures. It is clearly shown that the success rate decreases as the temperature is increased. The success of the device diminishes as the fault of the device is increased. The trends of the curves show both the thermal and fault tolerant characteristics of the device.

Fig.3.14(c) shows a decrease in success as the temperature increases. At 0, 1, 2, 3, 4, and 5 K, the OR 111 gate breaks down at a displacement factor of 0.250, 0.250, 0.250, 0.240, 0.260, and 0.055 respectively. From these BDF values one may state that the device is quite stable until the temperature rises to 4 K. One may also notice that at a temperature of 5 K, the device fails even with a slight defect.

A comparison of the OR gates is shown in Fig.3.15. It is a plot of the success rate versus displacement factors for the OR 101 and the OR 111 gates at absolute zero temperature. The defect tolerant characteristics of these two configurations at a fixed temperature are clearly observed from the two curves.

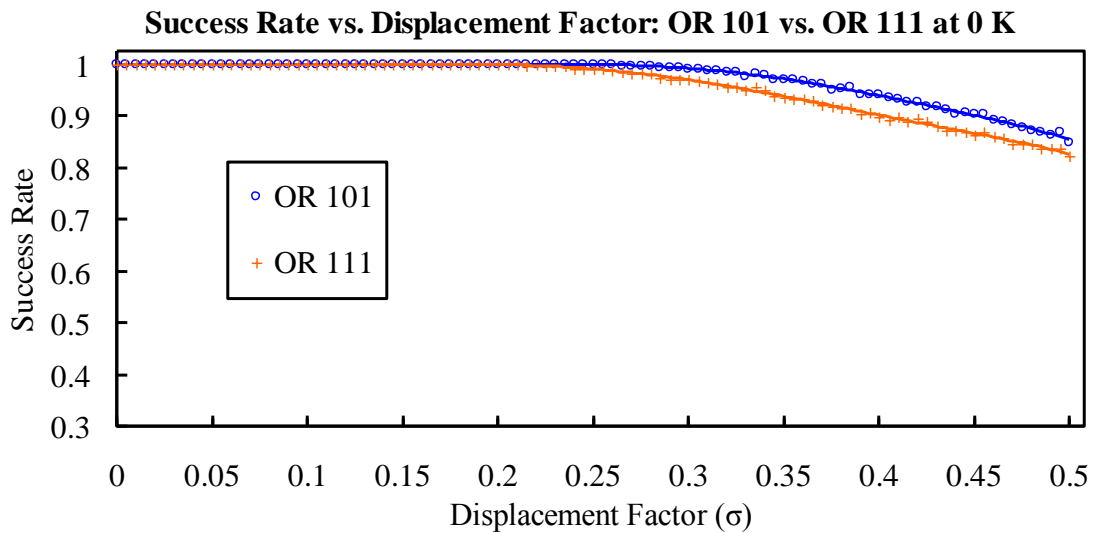


Figure 3.15: Comparison of Success Rate versus Displacement Factor for OR gates.

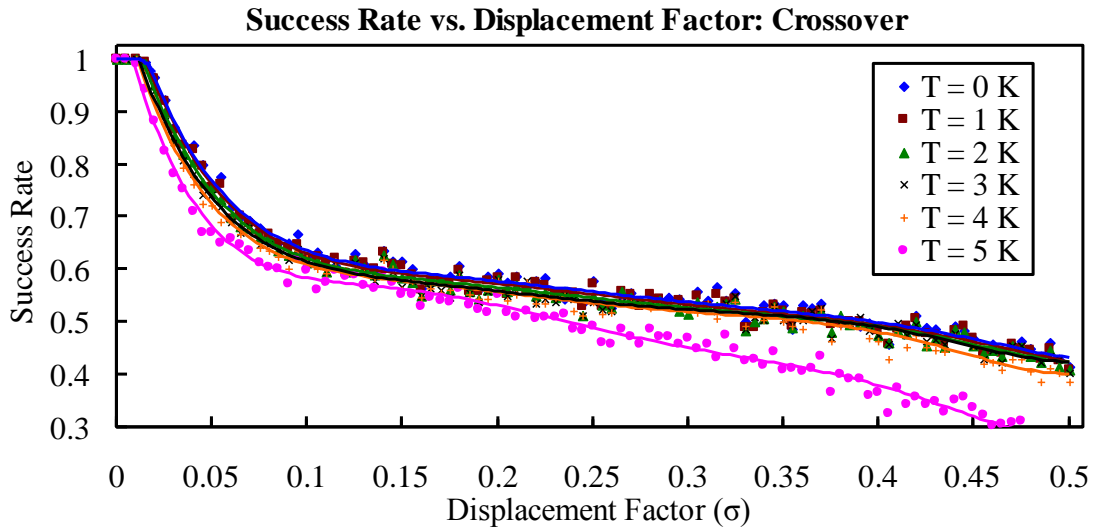
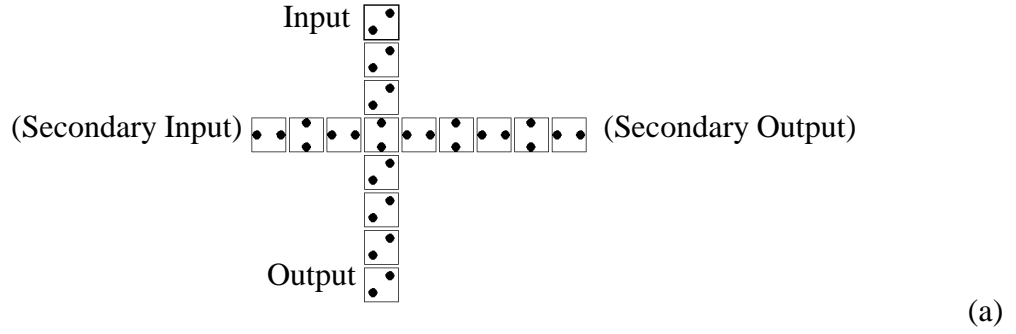
As mentioned above, the configuration of inputs can negatively interfere with the 5th cell. Intuitively, the OR 111 gate should outperform the OR 101 gate since all inputs are 1 instead of just two of the three. This is not how the gate actually performs. The interference of the matching top and bottom inputs (B and C) negatively influence the polarization of the 5th cell.

To summarize, the strongest majority gate tested is the OR 101 (= OR 001). The second strongest gate is the AND 110 (= AND 010). The third strongest is the OR 111 (= AND 000). The weakest majority is the AND 100 (= OR 011). The equivalency of all the cases is shown in Fig.3.7. All eight combinations of majority gates are reasonably close in functionality, and should be considered as equals for use in computations if manufactured to the worst-case (AND 100 or OR 011) specifications.

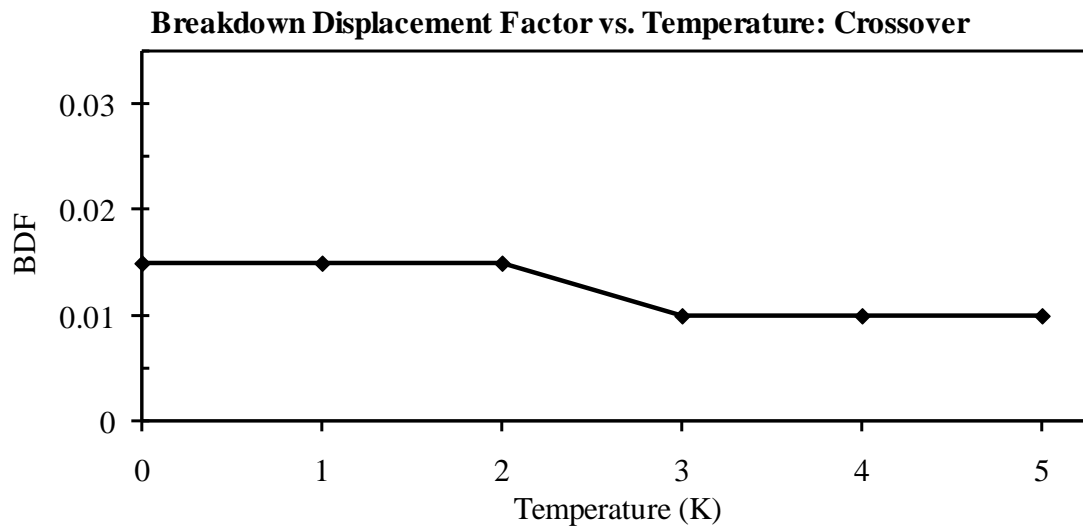
3.6. Crossover

In this planar scheme for computation, the simple task of crossing signals is not as simple as laying wires on top of each other. This seemingly simple gate is the one that creates the most problems. The signal propagation is based on near neighbor interactions, so as a wire is pulled apart to allow for another one to pass through, the other end of the wire becomes unstable.

One approach to constructing a crossover is to use a binary wire crossed with an inverter chain as shown in Fig.3.16(a). The theory is the rotated cells will have little influence on the side-to-side polarizations of the non-rotated cells, and vice versa.



(b)



(c)

Figure 3.16: The simulation results for a crossover: (a) The cell layout, (b) Success Rate versus Displacement Factor and (c) Breakdown Displacement Factor versus Temperature (Note the change in scale on the y-axis).

Fig.3.16(b) shows the success rate for the crossover at six different temperatures. This device performs very differently from the other basic devices, which was first observed by Anduwan [6]. It is shown that the device breaks down with very small displacement factors. There is still a lowering of success rate as temperature is increased, or as displacement factor is increased.

Fig.3.16(c) shows a slight decrease in success as the temperature increases. Note the $1/10^{\text{th}}$ change in scale on the y-axis as compared to the other device BDF curves. At 0, 1, 2, 3, 4 and 5 K, the crossover breaks down at a displacement factor of 0.015, 0.015, 0.015, 0.010, 0.010, and 0.010 respectively. Temperature has little effect since the device did not function properly even at 0 K, where it should have worked the best. Temperature does have a negative effect on QCA circuits, but the device has to work before additional temperatures can cause it to break down.

The crossover has proven to be much less stable than the other simple logic gates. This result is expected since the necessary Coulombic interactions require close proximity, which is absent for the vertical wire at the intersection of the two binary wires.

There have been a few different proposed ways to overcome the limitations of the crossover, but all include raising the complexity of the system, whether by introducing layers of cells [15] or by applying a bias voltage to act as a traffic light for the crossing signals [13].

3.7. Discussion

The above devices are the building blocks for more complex devices such as the XOR, full adder, comparator, Serial Bit-Stream Analyzer, memory device, etc... [1, 18,

19]. These basic devices have shown a clear temperature and defect dependence. It is clear in Fig.3.17 that the crossover is the least stable device. This is due to the lack of close proximity where the two signals cross. G. Anduwan realized the weakness of the crossover and declared it “not practical” as a QCA device [6]. This device will dominate the output of an Exclusive OR (XOR) design discussed in Chapter 4.

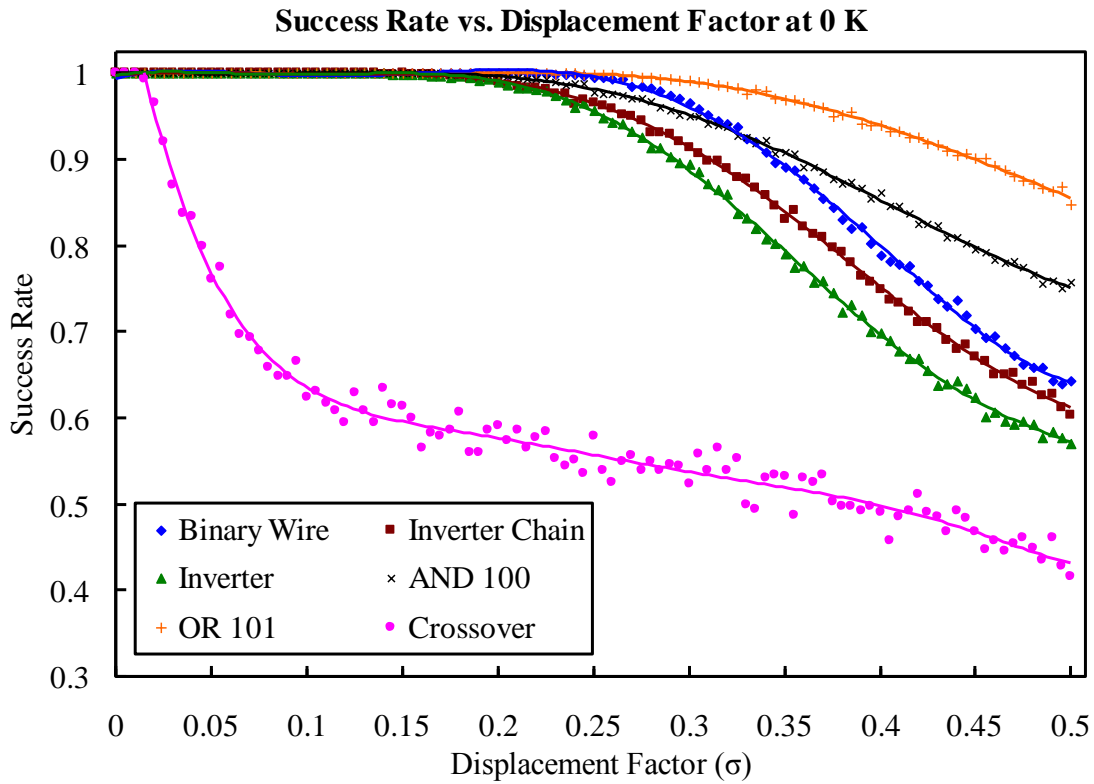


Figure 3.17: Summary of success rate versus displacement factor for all basic QCA devices at 0 K.

The other basic devices performed similarly with breakdown displacement factors ranging from 0.2 to 0.305 at 0 K as shown in Fig.3.18 and Table 3.1.

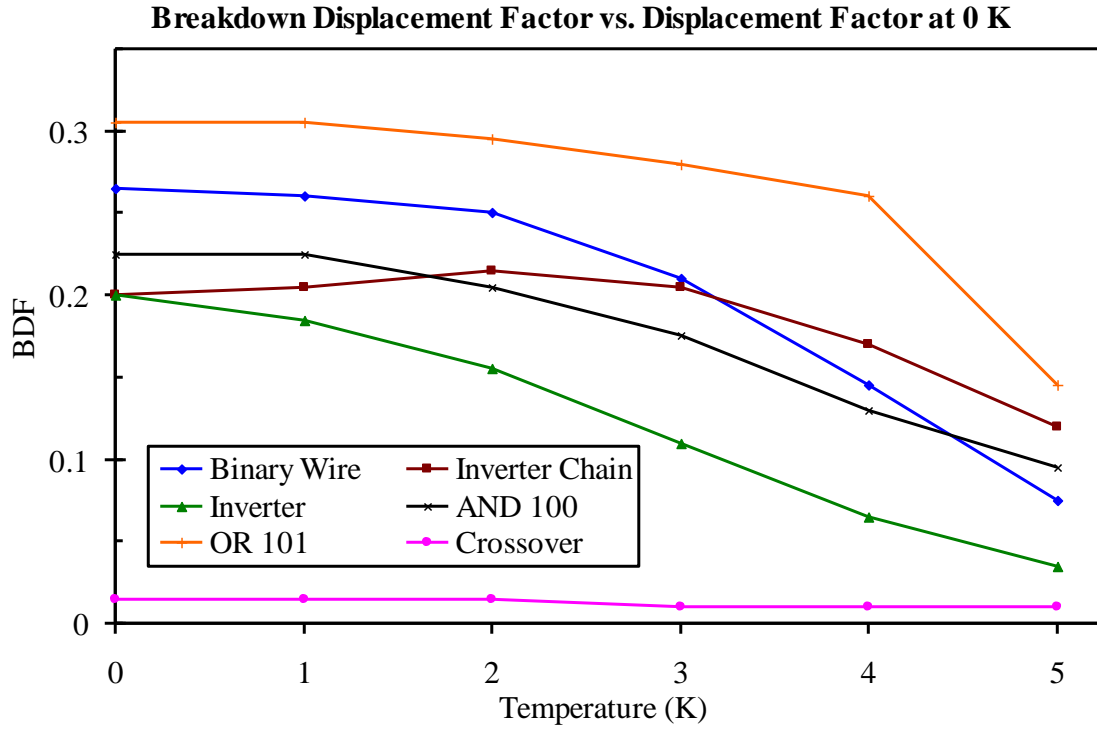


Figure 3.18: Summary of Breakdown Displacement Factors for all basic QCA devices.

Breakdown Displacement Factor (BDF)

Temperature:	0 K	1 K	2 K	3 K	4 K	5 K
Binary Wire	0.265	0.260	0.250	0.210	0.145	0.075
Inverter Chain	0.200	0.205	0.215	0.205	0.170	0.120
Inverter	0.200	0.185	0.155	0.110	0.065	0.000
Rotated-Cell Inverter	0.300	0.300	0.295	0.295	0.255	0.210
AND 100	0.225	0.225	0.205	0.175	0.130	0.005
AND 110	0.280	0.280	0.270	0.255	0.235	0.130
OR 101	0.305	0.305	0.295	0.280	0.260	0.145
OR 111	0.250	0.250	0.250	0.240	0.260	0.055
Crossover	0.015	0.015	0.015	0.010	0.010	0.010

Table 3.1: Summary of Breakdown Displacement Factors for all basic QCA devices.

The summary plots may make the OR gate seem more stable than the AND gate, but this is only due to the combinations of inputs tested. For example, the OR 011 gate would be just as unstable as AND 100 since their only difference is an arbitrary switch of polarization. Majority gate input redundancies are shown back in Fig.3.7.

All of the basic devices have been tested and show a strong correlation of success with temperature and dot displacement. With the basic devices investigated, we proceed to more complex circuitry in Chapter 4.

CHAPTER 4: THE EXCLUSIVE OR GATE

4.1. Introduction

An Exclusive OR (XOR) gate is similar to an OR gate, but outputs a 0 if both inputs are 1 as shown in the truth table in Table 4.1. This gate is relatively simple to create with traditional CMOS technology, but in the two-dimensional world of QCA, device fabrication difficulties arise. The XOR uses every basic device listed in Chapter 3. The truth table shown in Table 4.1 clearly shows that the QCA XOR device follows the Boolean logic from CMOS technology.

XOR Truth Table		
Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Table 4.1: Truth table for the XOR gate.

The Boolean logic for an XOR is $\overline{A}B + A\overline{B} = C$, so the device will require inverters, AND gates, an OR gate, binary wires to connect the gates, and a crossover to use both inputs twice. The traditional CMOS circuit diagram is shown in Fig.4.1.

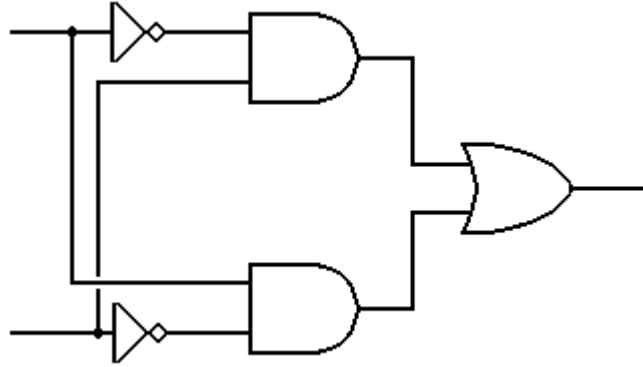


Figure 4.1: Traditional CMOS circuit diagram for an Exclusive OR gate.

4.2. The 64-Cell Design Exclusive OR Gate

D. Tougaw introduced the 64-cell QCA design for an XOR shown in Fig.4.2 [1]. In order to utilize the crossover, the top input must be offset by half of a cell spacing. This offset will invert the signal, which is inverted back after the crossover by another offset junction. Then that same signal is inverted yet again by an inverter before reaching the bottom AND gate. It is a cumbersome design, but necessary to adapt the XOR to the QCA system.

Due to a large requirement of computational resources, only temperatures of 0 K to 3 K were extensively tested for each of the four sets of inputs; $AB = 00, 01, 10, 11$. Results of fault tolerant characteristics and thermal behavior on the operation of different input configurations are discussed below. In the simulation, the total number of displacement factors used is 50, and for each displacement factor 2000 trials are used.

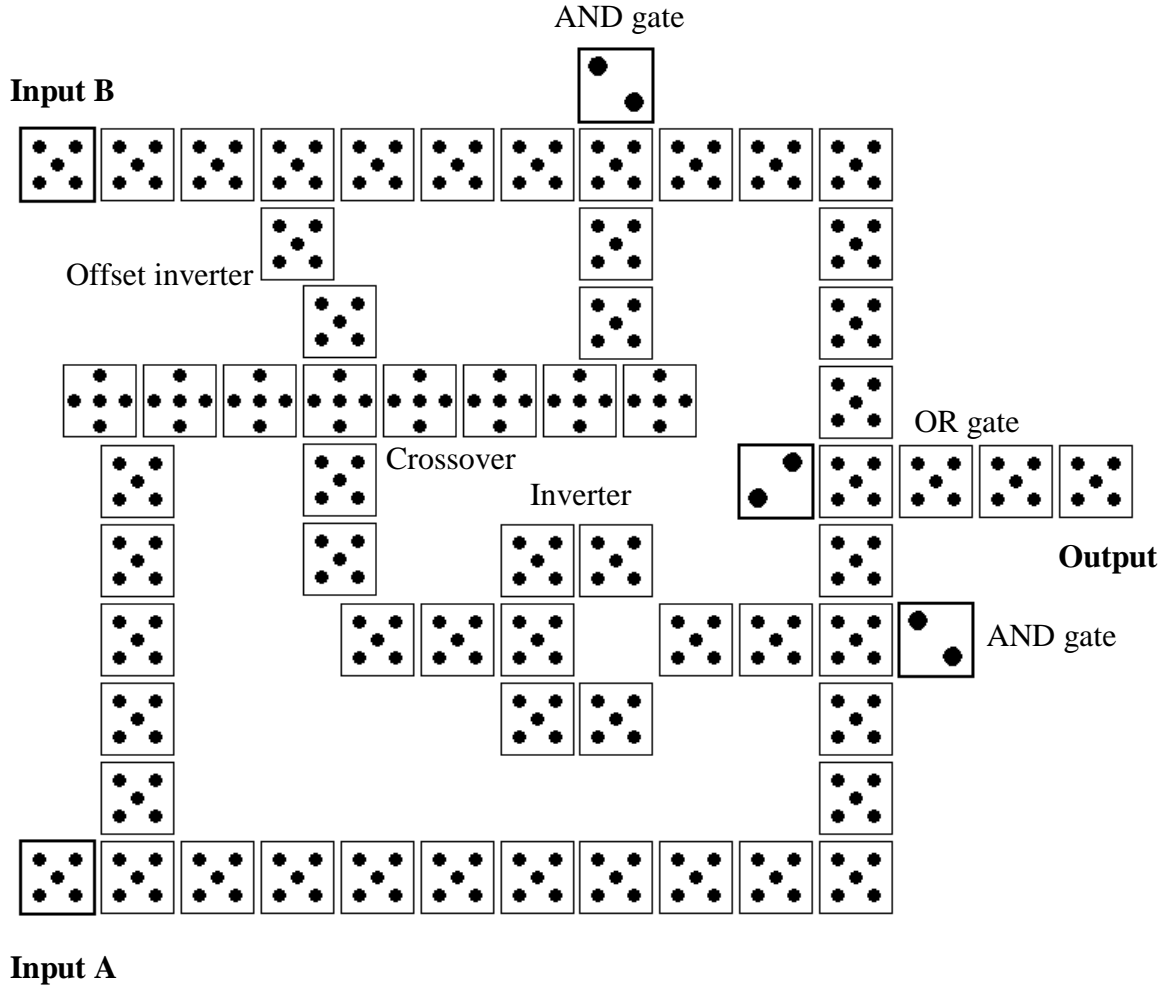


Figure 4.2: The 64-Cell XOR design was simulated using 2000 trials over 50 displacement factors.

The first inputs of the XOR gate to test are $AB = 00$. The layout of the XOR 00 gate is shown in Fig.4.3(a). For this combination of inputs, both paths of the crossover are not important since the majority gates they lead to already have the majority decided.

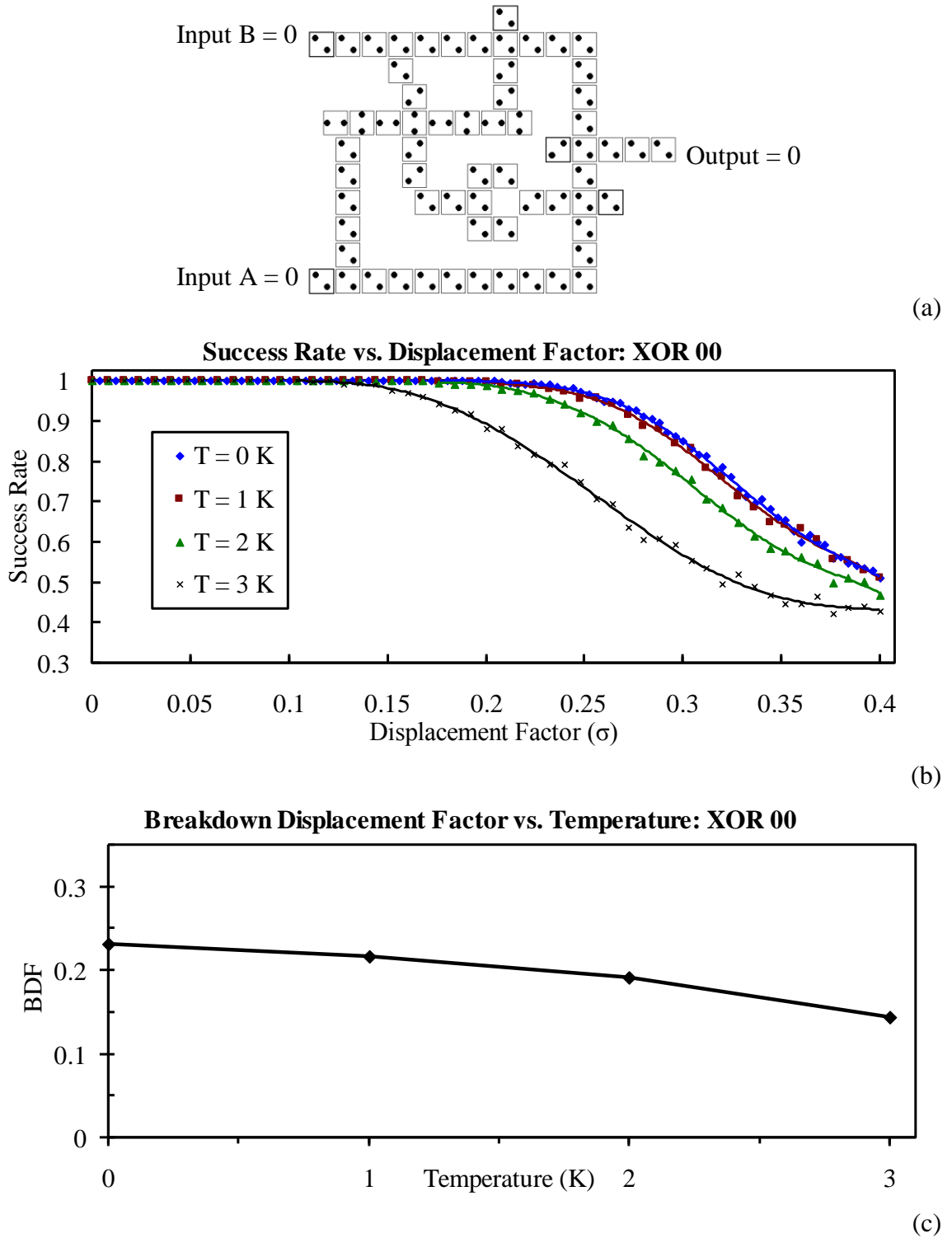


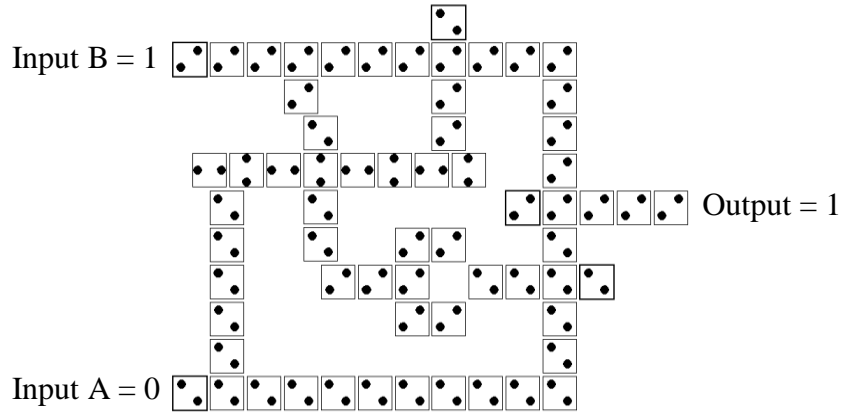
Figure 4.3: The XOR 00 gate (a) layout, (b) Success Rate versus Displacement Factor at $T = 0, 1, 2$ and 3 K, and (c) Breakdown Displacement Factor versus Temperature.

Fig.4.3(b) shows the success rate as a function of displacement factor for the XOR 00 gate. The general features of the curves are similar to the basic QCA devices discussed in Chapter 3. In order to avoid the long and the tedious simulation, results are produced for only four different temperatures: $T = 0, 1, 2$, and 3 K. As the temperature is increased, the device starts to fail at smaller displacement factors.

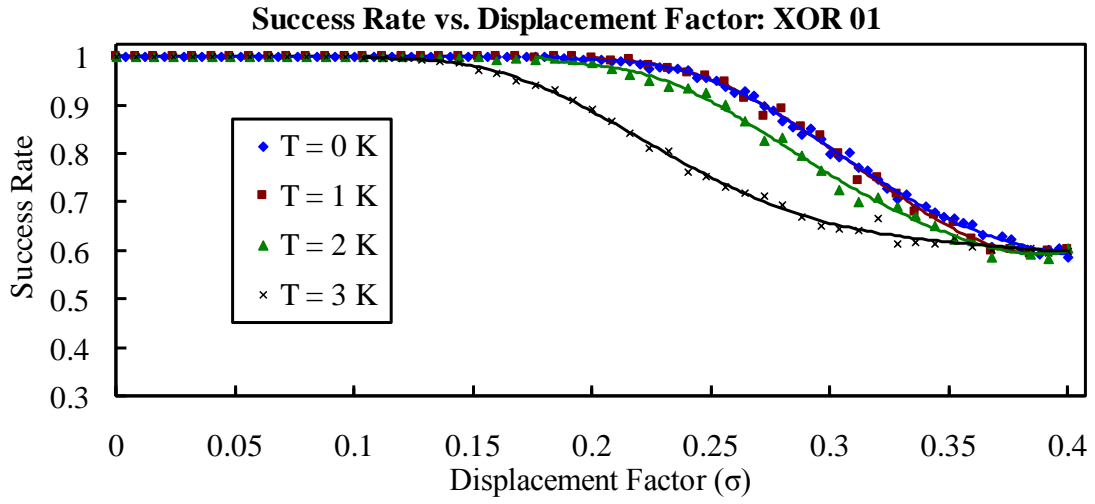
Fig.4.3(c) shows the BDF values as a function of temperature. For each increase in temperature, the BDF values decrease. At $0, 1, 2$ and 3 K, the XOR 00 gate breaks down at displacement factors of $0.232, 0.216, 0.192$, and 0.144 respectively.

The results for the XOR 01 gate are presented in Fig.4.4. The device layout is shown in Fig.4.4(a). For this combination of inputs, only the top AND gate needs a strong signal from the crossover since the fixed majority gate input and input B do not match. The success rate as a function of displacement factor is plotted for four different temperatures, $T = 0, 1, 2$ and 3 K in Fig.4.4(b).

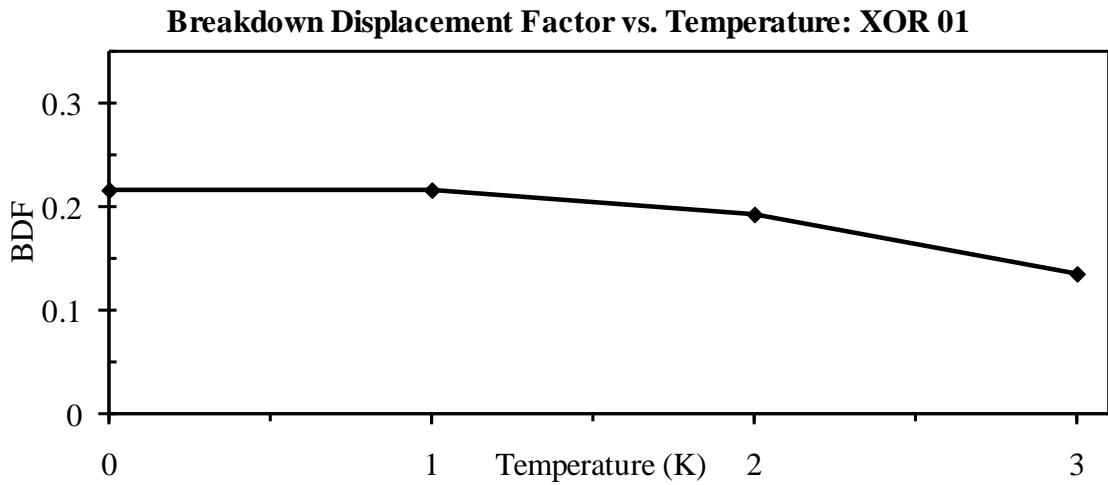
The trends of the graphs are similar to the XOR 00. The device starts to fail systematically at different defect parameter values as the temperature is changed. There is almost no temperature effect from 0 to 1 K. At 2 K and 3 K, the curves depart from the lower temperatures and operate poorer. The breakdown displacement curve in Fig.4.4(c) displays a comprehensible picture of the thermal and defect tolerant features of the XOR 01 device.



(a)



(b)



(c)

Figure 4.4: The XOR 01 gate (a) layout, (b) Success Rate versus Displacement Factor at $T = 0, 1, 2$ and 3 K, and (c) Breakdown Displacement Factor versus Temperature.

Next, the results for the XOR 10 gate are discussed. The device layout is presented in Fig.4.5(a). For this configuration, the bottom AND gate needs a strong signal from the crossover and inverters to break the tie between the fixed majority gate input and input A. As for the other devices, the defect and thermal tolerance behavior of the device are studied using the success rate and the displacement factor defect parameter. Fig.4.5(b) exhibits the success rate of the device as a function of displacement factor for four different temperatures, $T = 0, 1, 2,$ and 3 K, but with a change in scale.

One may notice that the range of the horizontal axis in Fig.4.5(b) lies between 0 and 0.1, whereas the range of the horizontal axis for the above XOR devices is between 0 and 0.4. The XOR 10 gate is very sensitive to the presence of a defect of any magnitude. Almost all of the curves in the figure start to drop from the value of unity (full success) at a very small displacement factor value, and the curve for 3 K breaks down at the ideal condition of no dot displacement. The BDF values for all temperatures are at or below 0.02 as shown in Fig.4.5(c). Again, note the one tenth change in scale on the BDF axis. At 0, 1, 2 and 3 K, the XOR 10 gate breaks down at displacement factors of 0.018, 0.020, 0.014 and 0.000 respectively. From these low BDF values one may predict that the 64-cell XOR design is not suitable for operation with $A = 1$ and $B = 0$ inputs. The cause of the sensitivity and the failure of the device with this specific input configuration are explained at the end of this section.

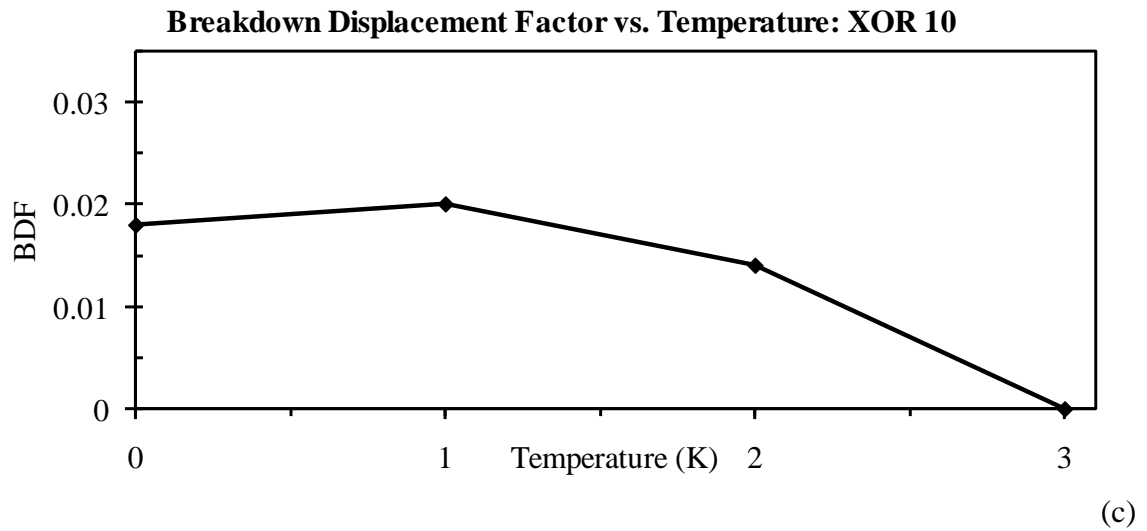
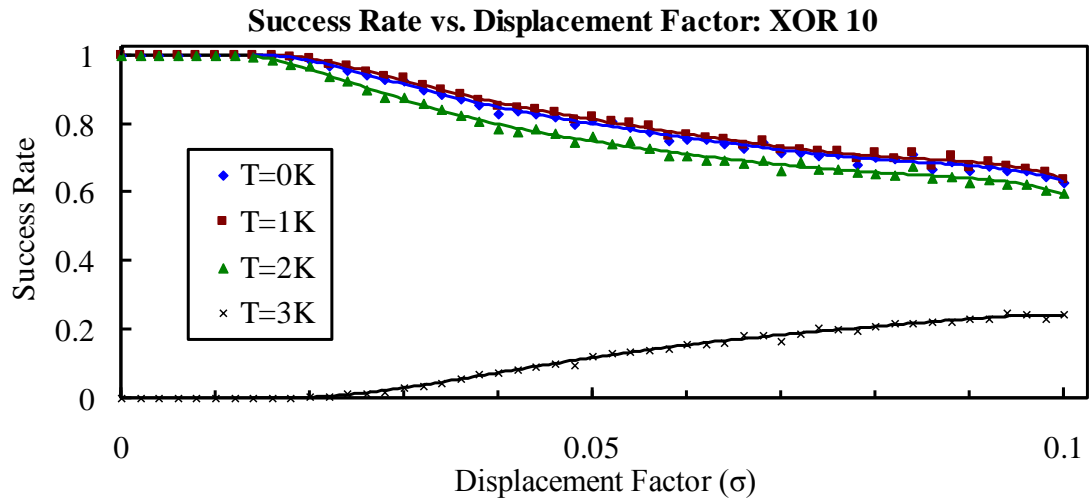
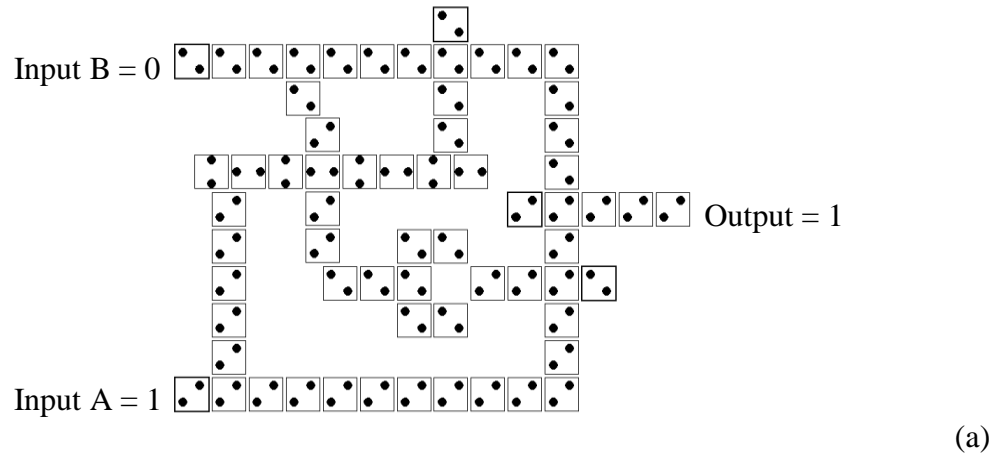


Figure 4.5: The XOR 10 gate (a) layout, (b) Success Rate versus Displacement Factor at $T = 0, 1, 2$ and 3 K, and (c) Breakdown Displacement Factor versus Temperature.

Finally, the XOR 11 gate results are discussed. The device layout is shown in Fig.4.6(a). The success rate versus displacement factor plots are shown in Fig.4.6(b). Again, note the change in scale. For this device, only the results from the range 0 to 0.1 displacement factor are shown to show detail of the breakdown points. The device can function with small defect only at 0 K. For temperatures above 0 K, any dot displacement causes the device to fail. At 3 K, the device cannot function.

Fig.4.6(c) shows that the BDF values are near zero at all temperatures. One may conclude from the investigation in this thesis work that the XOR 11 input configuration is the most sensitive to defect. It is predicted that for the XOR input configurations of 10 and 11, the 64-cell XOR design shown in Fig.4.2 will not operate properly. There is a fundamental weakness in the design. The detailed explanation is given below.

Now that all of the XOR input combinations have been presented, we move on to discussion of the results. To reduce clutter, only the thermal and fault tolerant characteristic results of the XOR device at 0 K are described and presented in Fig.4.7.

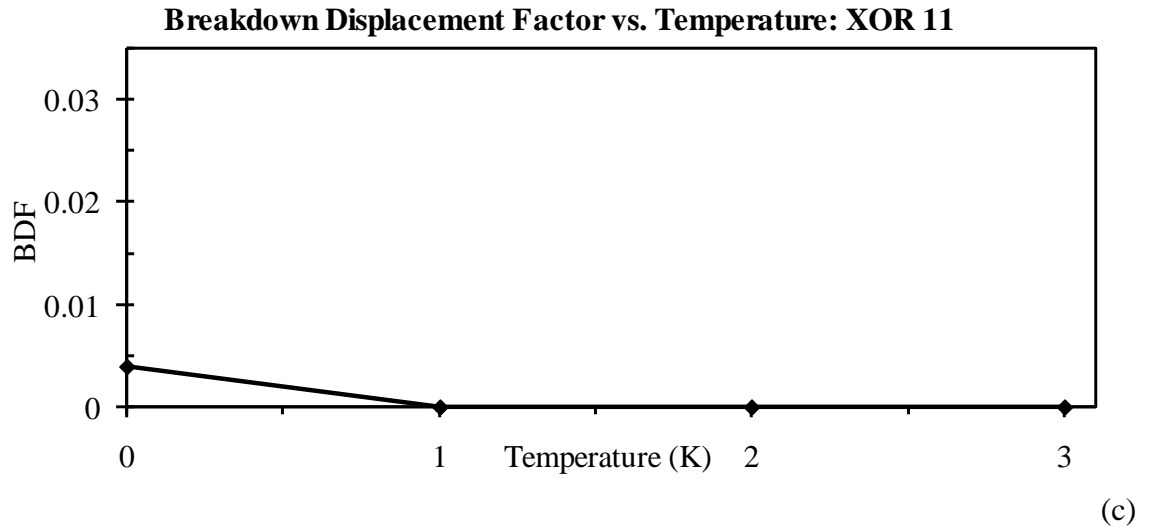
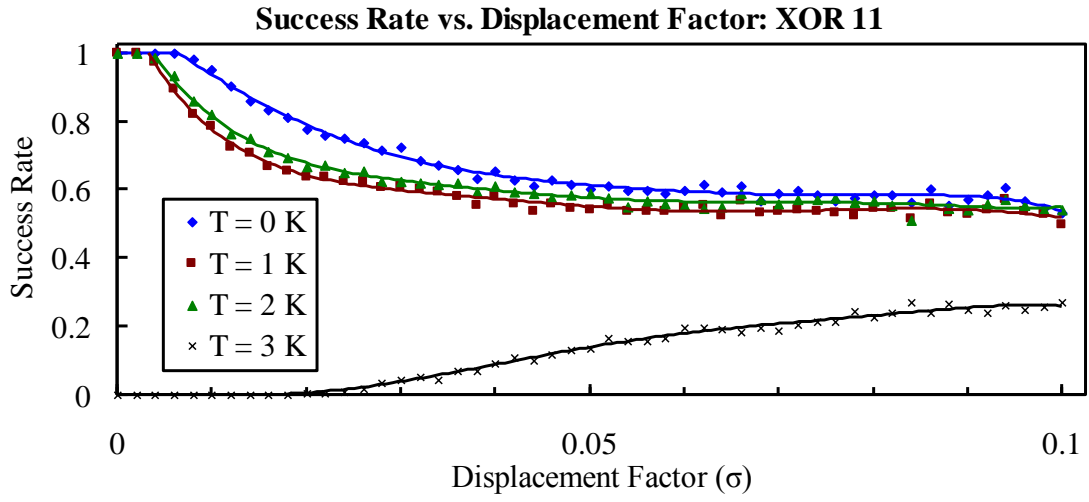
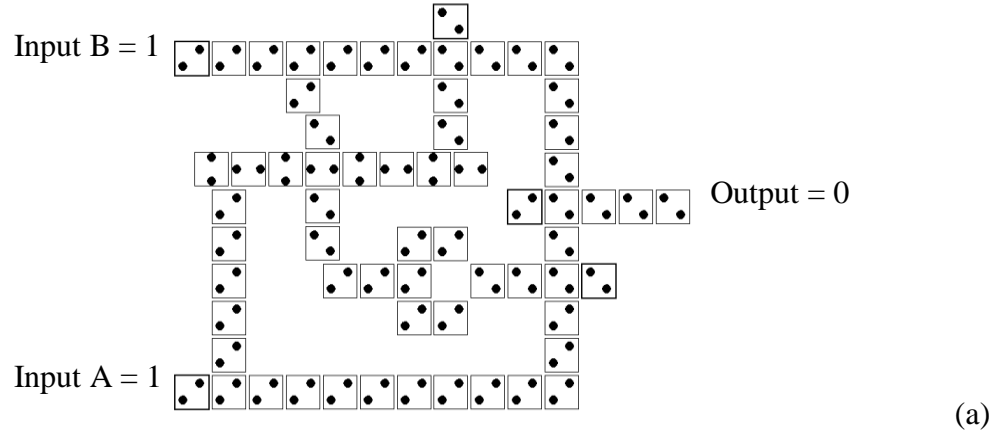


Figure 4.6: The XOR 11 gate (a) layout, (b) Success Rate versus Displacement Factor at $T = 0, 1, 2$ and 3 K, and (c) Breakdown Displacement Factor versus Temperature.

The success rate versus displacement factor is plotted for all of the XOR input combinations. The inputs 00 and 01 show similar results to the basic logic gates, but the inputs 10 and 11 are clearly much less stable. After much trouble-shooting and investigation, the difference was determined to be due to the inclusion of the crossover.

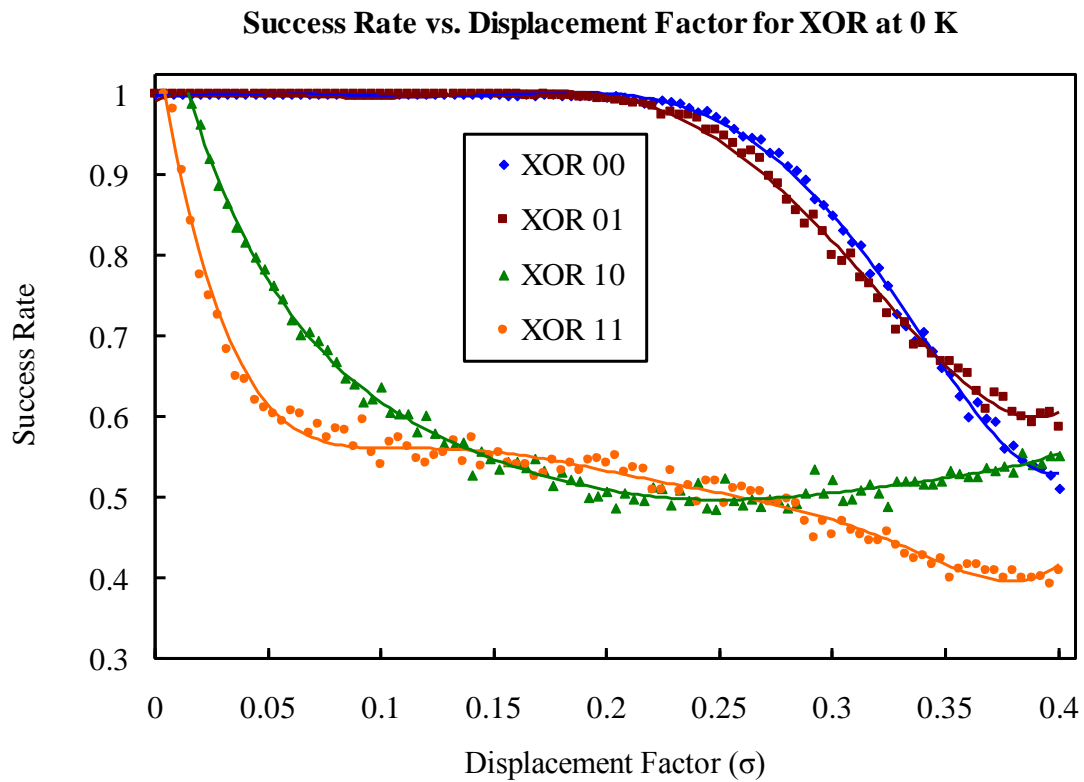


Figure 4.7: The simulation results for D. Tougaw's 64-cell XOR design: Summary of Success Rate versus Displacement Factor.

The presence and the impacts of the crossover on an XOR will be discussed here. In order to get a strong signal from the AND gates (with a fixed 0 input) one should put emphasis on the fact that both incoming signals from the inputs A and B must provide adequate impact to override the fixed input when necessary. If the incoming signals are

not strong enough for the AND gate to operate properly, the gate cannot produce a strong outgoing signal for the next stage in the device.

Here, the discussion concentrates on the bottom AND gate on the right most vertical line in Fig.4.2. For the XOR 00 and the XOR 01 the first input, 0, reaches the bottom AND gate by passing through the bottom binary wire. This signal is less interfered by other cells and components of the device. This input and the fixed 0 input on the AND gate override whatever comes through the crossover. Thus, the AND gate produces a strong signal for the next stage for computation in the device.

On the other hand, for the XOR 10 and the XOR 11, the first input 1 will arrive to the bottom AND gate through the binary wire similar to the other two situations discussed above. The strong 1 will combine with the fixed 0 of the AND gate and require the inverted input B signal to break the tie in the majority gate. Since input B must travel via the sensitive crossover, the signal that reaches the bottom AND gate may not be strong enough to consistently produce the correct output. In this circumstance, the effect of temperature seems to be irrelevant.

Fig.4.8 displays the summary of the breakdown displacement factors as a function of temperature. The BDF values for the XOR 00 and the XOR 01 are comparable at all four temperatures. Similarly, the BDF values for the XOR 10 and the XOR 11 are nearly identical. Both the XOR 10 and XOR 11 will fail to operate with an infinitesimal dot displacement defect, even at absolute zero temperature.

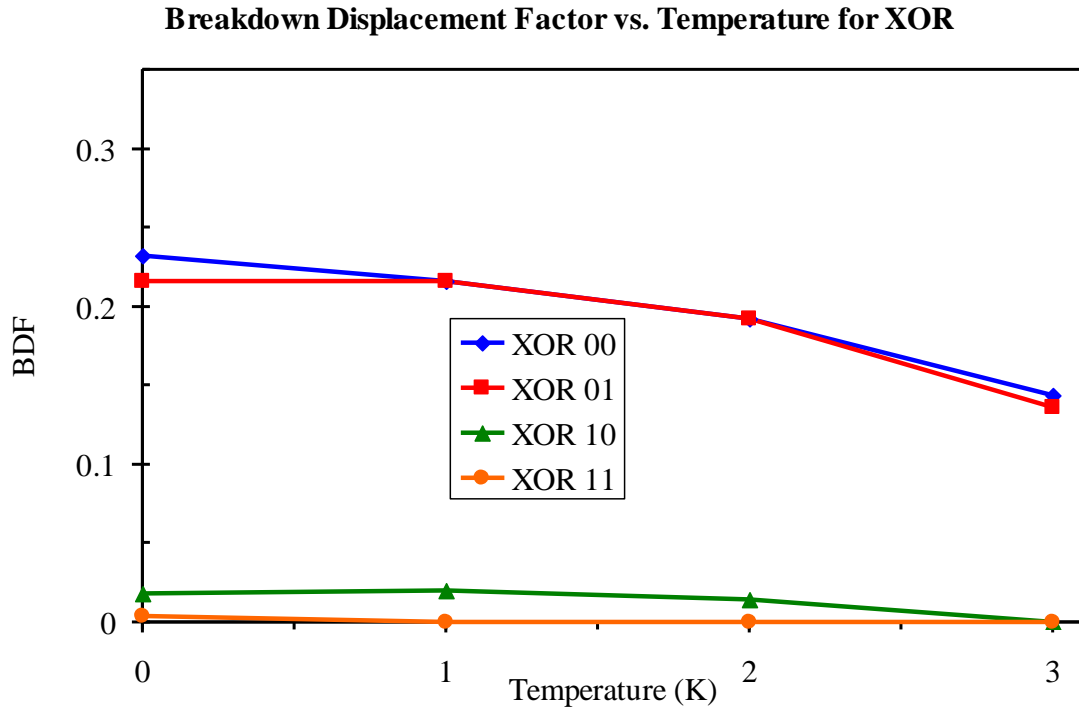


Figure 4.8: The simulation results for D. Tougaw's 64-cell XOR design: Summary of Breakdown Displacement Factor versus Temperature.

To test the hypothesis that the crossover is indeed the device causing the instability in the XOR, a comparison of XOR and the crossover was produced in Fig.4.9 and a comparison of their breakdown displacement factors is shown in Table 4.2. The XOR 10 curve is almost identical to the crossover curve. The XOR 11 is a little less stable than the crossover due to both AND gates requiring a strong signal from the crossover to produce the correct majority outputs.

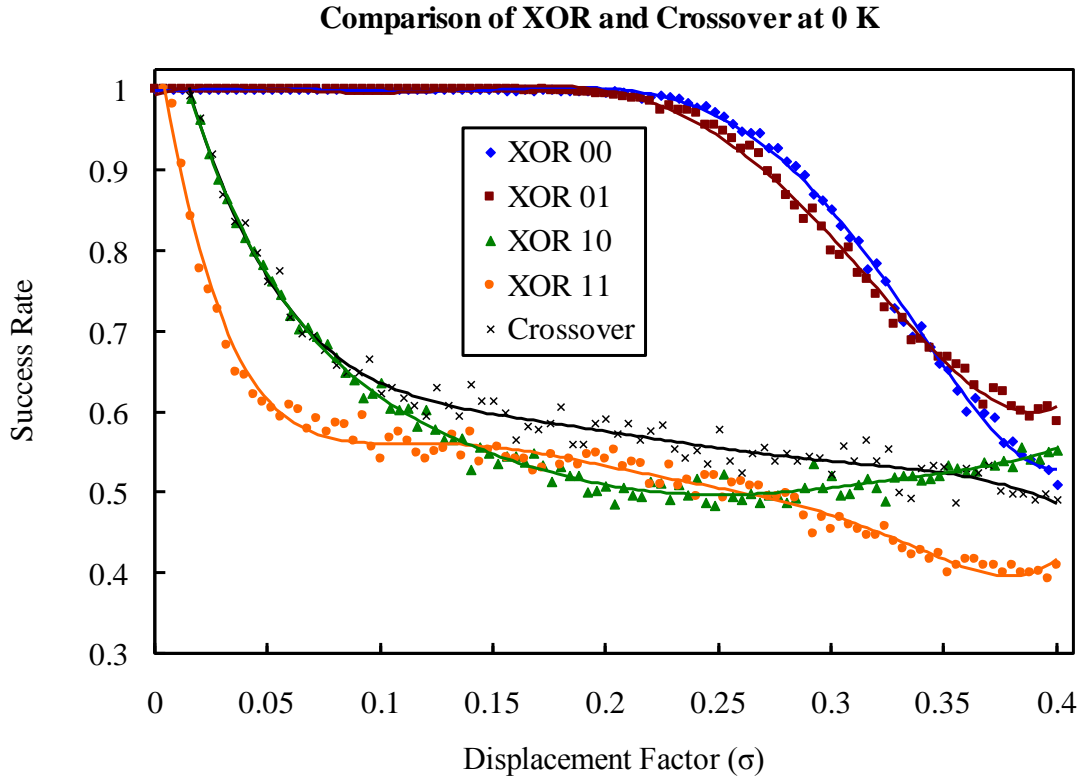


Figure 4.9: Comparison of the XOR and the crossover Success Rate versus Displacement Factor at 0 K.

Breakdown Displacement Factor (BDF)

Temperature:	0K	1K	2K	3K
XOR 00	0.232	0.216	0.192	0.144
XOR 01	0.216	0.216	0.192	0.136
XOR 10	0.018	0.020	0.014	0.000
XOR 11	0.004	0.000	0.000	0.000
Crossover	0.015	0.015	0.015	0.010

Table 4.2: The Breakdown Displacement Factors for the XOR and the Crossover.

At a displacement factor of 0.3, the XOR 10 and XOR 11 begins to diverge in Fig.4.9. This is simply due to weak inputs reaching the ending OR gate. If the OR gate inputs are not strong enough, the fixed OR gate input of 1 will dominate regardless of the rest of the device. The expected output for the XOR 10 is a 1, which the under-restricted OR gate shoves through to the output, thus creating a “successful” trial. It should not be considered an actual success since the device came to the correct output by failing. For the XOR 11, the expected output is a 0, but again the OR gate again asserts its fixed 1 to the output of the XOR and causes an unsuccessful trial.

4.3. The 57-Cell Design

The weak point of the above 64-cell XOR design [1] has been determined to be the crossover. To improve upon the functionality of the crossover, the vertical path was doubled up. After improving the crossover, the rotated-cell inverter was incorporated to reduce the size of the gate and the number of cells used. These modifications lead to the new 57-cell XOR design as shown in Fig.4.10.

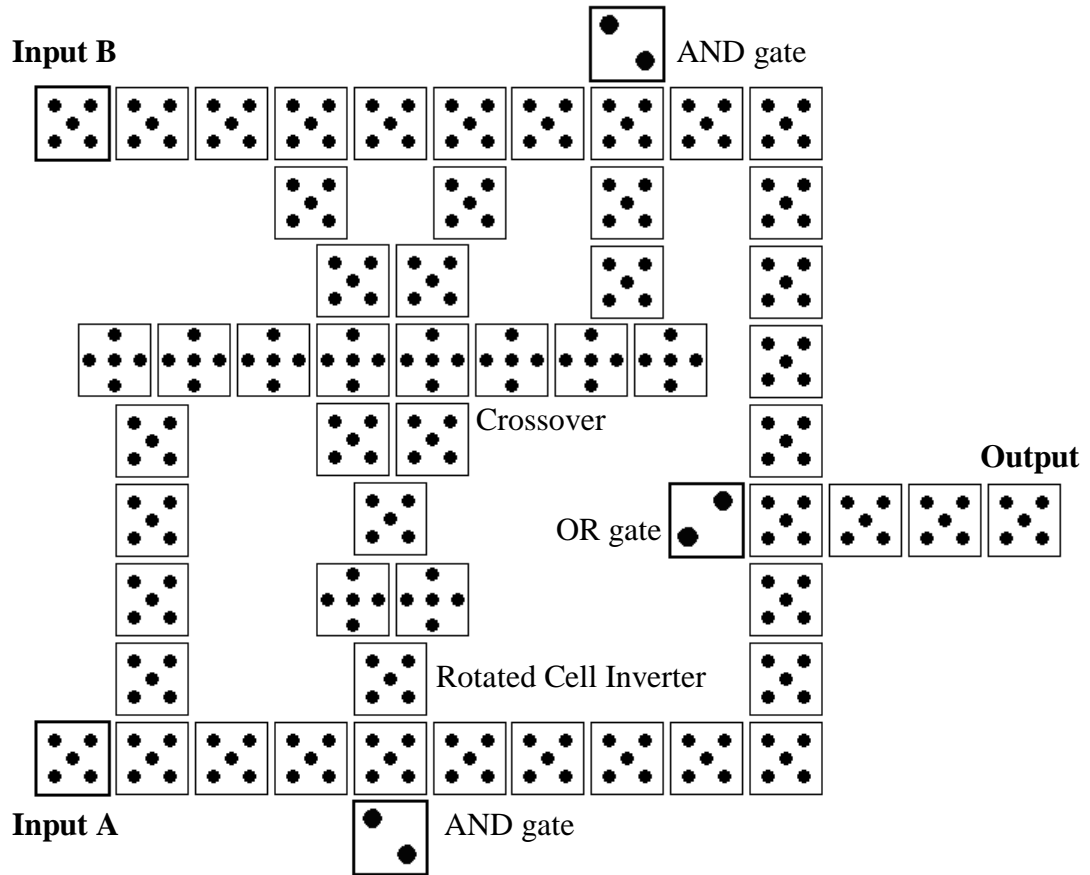
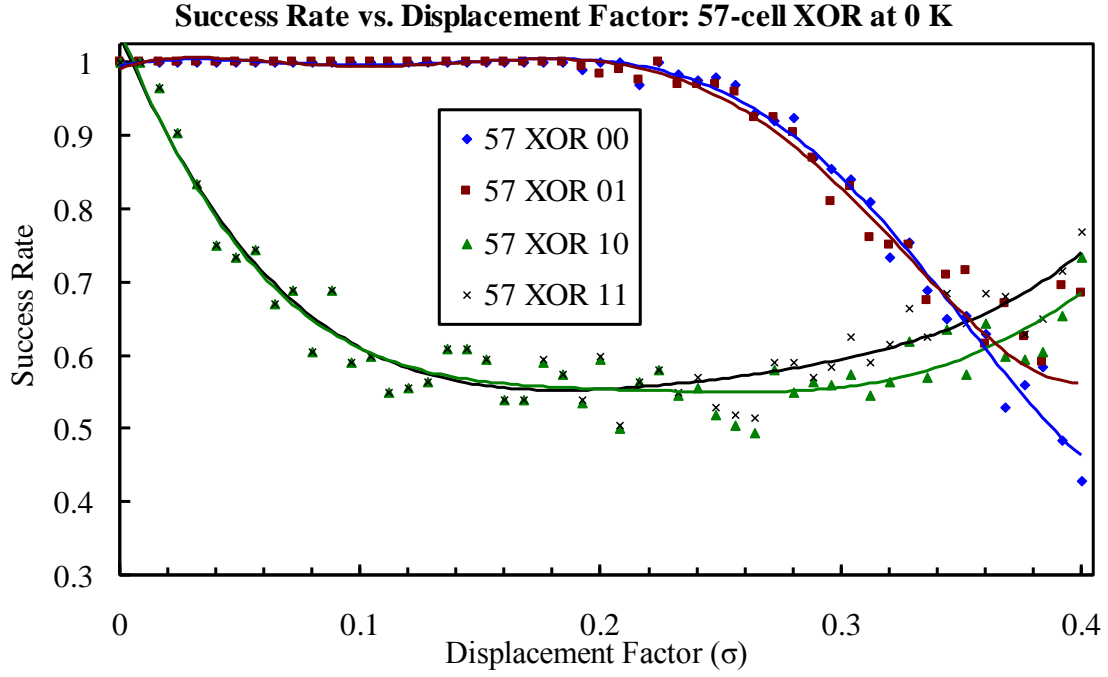
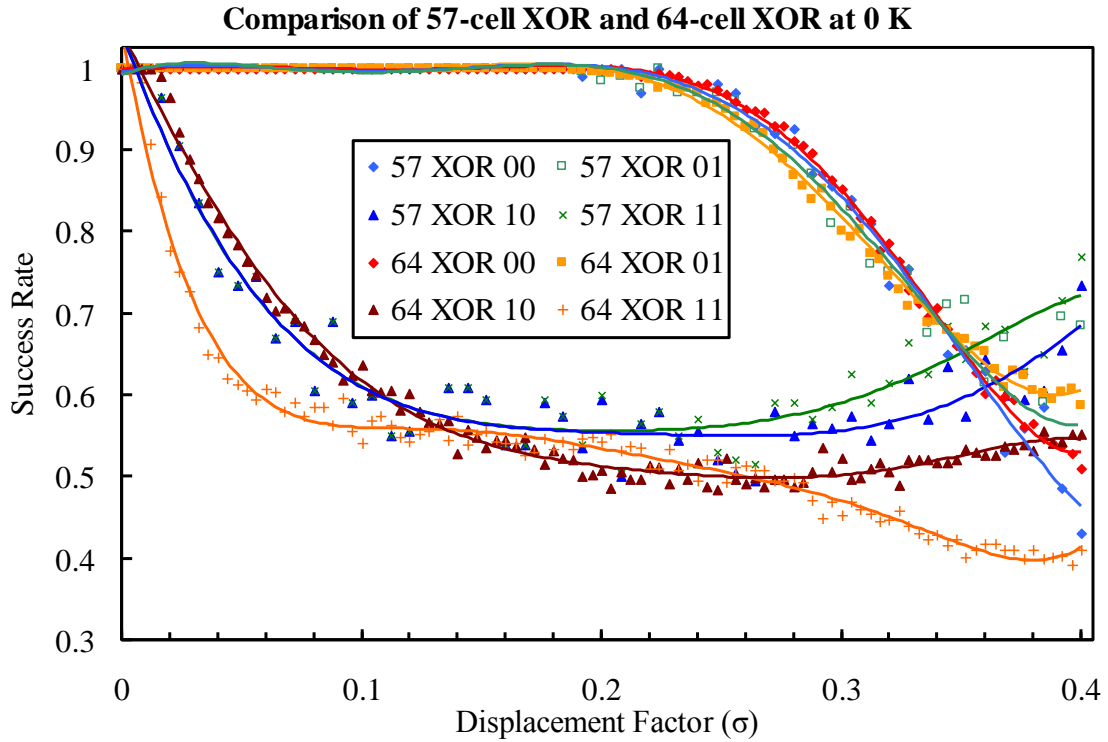


Figure 4.10: The cell layout for the 57-cell XOR design.

The results for the new design are seen in Fig.4.11(a). The new design does not improve the success rate enough to consider the gate functional, but it does improve slightly while using fewer cells as shown by the comparison in Fig.4.11(b). The results indicate the crossover is still the weakest portion of the XOR design. To construct a functional XOR, either vertical inputs could be used to avoid crossing signals, or the use of clocking could be introduced as described in section 4.4.



(a)



(b)

Figure 4.11: The simulation results for the 57-cell XOR design: (a) Success Rate versus Displacement Factor and (b) Comparison to 64-cell XOR design at 0 K.

4.4. Clocked XOR Design

To completely overcome the shortcomings of the crossover, it needs to be completely eliminated. In order to cross signal paths without a crossover, there needs to be a tool to control the traffic of signals. That tool is clocking.

Clocking works by controlling a bias voltage applied to the underside of a QCA device. By increasing the voltage, tunneling energy is decreased, thus locking a cell to one polarization. By dropping the voltage, tunneling energy is increased and the cell can easily switch polarization [13].

The clocked XOR design shown in Fig.4.12 uses more cells than the unclocked designs, but this is to allow for crossover timing. Without the added path lengths, the signals would cross at the same time and the crossing binary wires would act as a two-input majority gate, rendering the XOR useless.

This device has yet to be simulated due to the added difficulty of clocking. Each component has been tested individually without clocking, and clocking will only improve operation [13]. Clocking has been shown to be a viable resource [20], so there is little doubt in the clocked XOR functionality.

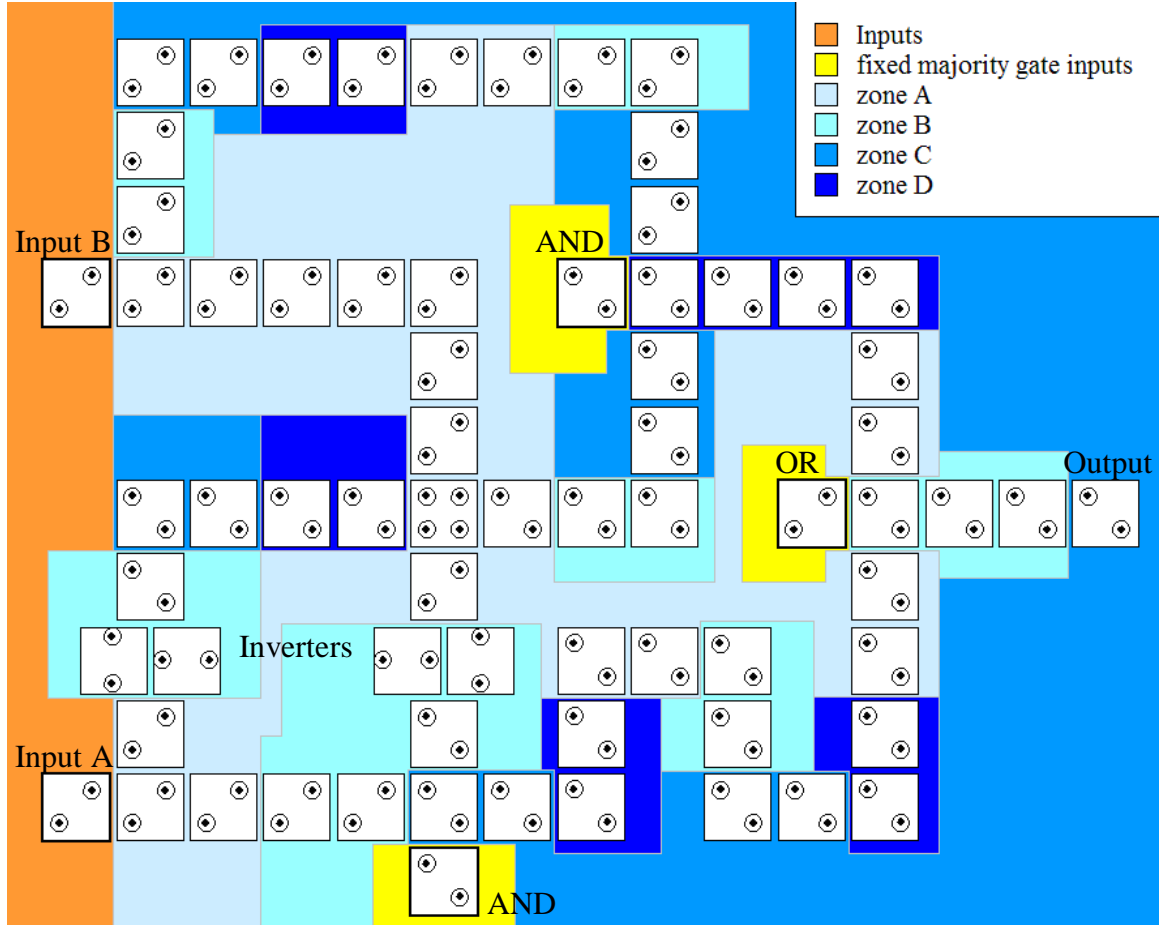


Figure 4.12: 71-cell clocked XOR design with inputs 1, 1 and output 0.

4.5 Discussion

For the XOR device, the main obstacle to overcome is the crossing signals. Initial designs incorporated the crossover, which has been shown to be overwhelmingly the weakest basic device in Chapter 3.

Attempts were made in the current thesis work to improve the functionality of the crossover in the XOR design. Even with these modifications, the crossover still proved to be the weak link in the design, and would need to be eliminated for an XOR to be a feasible QCA device.

The need for the crossover has been eliminated with the introduction of clocking. Clocking allows for control of signal flow. Instead of crossing two signals simultaneously, one direction is allowed to pass while the next signal waits to pass. Once the first signal has passed through, the cells are relaxed again. Once the cells are fully relaxed, the next signal can cross without interference or residual polarization. With this scheme, the crossing paths are like two separate binary wires with one shared cell, thus the success should be approximately the same as the binary wire presented in Chapter 3, but with the added stability benefit that clocking adds [13, 20]. Clocking solves the problems of XOR, and can also be applied to other complex devices that struggle with crossing signals.

CHAPTER 5: CONCLUSIONS

5.1. Summary

The basic logic gates and the XOR gate have been simulated. All of the basic devices except for the Crossover function within a displacement factor of 0.200 at 0 K, to a displacement factor of 0.035 at 5 K. The Crossover has a small fault tolerance of 0.015 to operate at 0 K.

The 64-cell XOR design can operate within the fault of 0.216 displacement factor at 0 K if input A is a 0, but the fault has to be reduced to 0.004 to operate for any combination of inputs.

The 57-cell XOR design increased the available fault tolerance to 0.224 at 0 K if input A is 0, or a fault tolerance of 0.008 for any combination of inputs. This design uses 7 less cells with slightly improved results compared to the 64-cell XOR design. It is not a complete success, but still an improvement.

The clocked XOR design should work, but still needs testing to prove so. The individual components that make up the clocked XOR have all been tested without clocking, and clocking should only improve their performance, so there is little doubt the clocked XOR will fail.

5.2. Conclusions

The temperature and defect dependence of QCA devices have been studied. The binary wire, inverter chain, inverter, AND, OR, crossover, and XOR have been investigated. A systematic behavior has been observed for all devices except for the crossover and XOR. The success rate decreases with increased temperature and dot displacement for all devices. Results show the crossover is extremely sensitive to any magnitude of defect and temperature. The results of the XOR device indicate it inherits the sensitive behavior of the crossover, especially when the crossover output is needed in a majority gate (XOR inputs 10 and 11).

The current simulated QCA system is only stable at very low temperatures, so benefits over traditional CMOS are outweighed by its disadvantages. The reduced size and power usage of the processor is irrelevant when the cooling system would make the total computer much larger and energy hungry. With the large cooling requirements, this model would be best suited to space travel [1]. QCA would reduce the size and weight of the onboard computers, reduce energy requirements, and would be stable at the ambient space temperature of around 2.7 K.

5.3. Future Work

The current thesis work is merely a start to the research needed to determine the feasibility of QCA as a worthy replacement to present CMOS technology. In addition to dot displacement, investigations need to be performed on cell displacement, missing dots, and missing cells. Then clocking would need to be explored as well, for both the four

and five dot QCA models. But even with no defect, the current model is only functional at very low temperatures.

To improve the temperature sensitivity, the model would need to be reduced to the molecular scale. As confinement is increased to the molecular scale, the energy states raise well above room temperature. If self-assembly can be utilized, the benefits become even stronger. [21, 22]

Additional work needs to be done to improve the strength of the crossover. One possible solution is to move away from the traditional planar scheme and utilize vertical inputs [6, 15]. Moving QCA from a planar system to a multi-level scheme would allow for much more intricate circuitry with fewer cells.

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